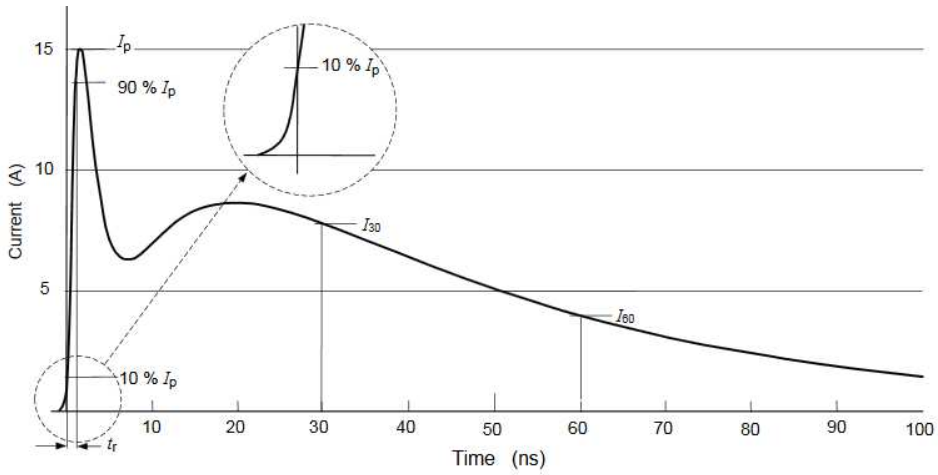
EMC Problem

Protecting a digital input against electrostatic discharge (ESD)

Electrostatic discharge (ESD) is a huge concern for integrated circuits as a source of soft and hard failures. ESD is due to charge transfer from human body or any insulated device to an electronic device. ESD appears during IC assembly process, but also during the operation of electronic system. In general, ESD at system level are more energetic than those observed during assembly process. To prevent IC damage during assembly process, ESD protections are placed on each IC terminal. They trigger if fast transient overvoltage conditions arise on IC terminal, limit the voltage applied on IC terminal and deviate the discharge current through a low impedance path.

However, ESD protections at IC level may be insufficient to protect the circuit at system level and may be destroyed due to oxide breakdown or thermal stress, leading to IC damage. Thus, equipment designers have to place external protection elements to limit the residual transient pulse that reaches IC terminal. The purpose of this problem is to learn how to protect IC terminal against ESD at printed circuit board level.

In this problem, the considered ESD waveform complies with the IEC61000-4-2 standard, whose typical waveform is given by the following figure. For test purpose, ESD stimulator or ESD gun are developed and respond to this standard.



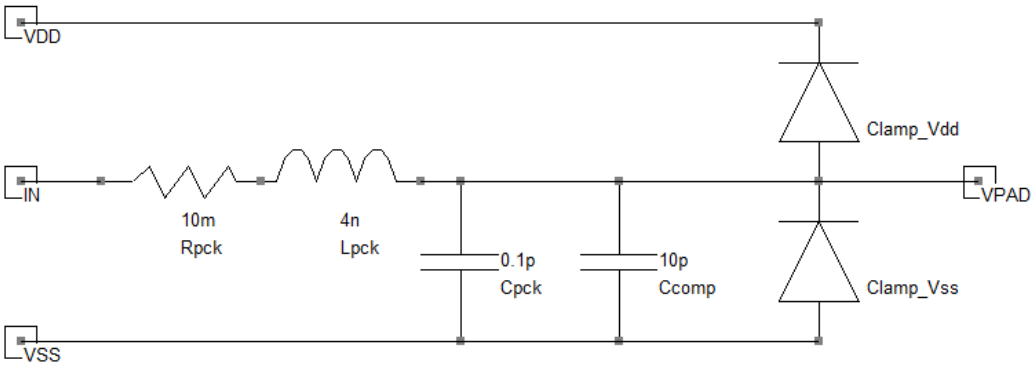
Ideal contact discharge current waveform at 4 kV (2 ohms)

Table 3 – Contact discharge current waveform parameters

Level	Indicated voltage kV	First peak current of discharge ±15 % A	Rise time t_r (±25 %) ns	Current (±30 %) at 30 ns A	Current (±30 %) at 60 ns A
1	2	7,5	0,8	4	2
2	4	15	0,8	8	4
3	6	22,5	0,8	12	6
4	8	30	0,8	16	8
The reference point for measuring the time for the current at 30 ns and 60 ns is the instant when the current first reaches 10 % of the 1st peak of the discharge current. NOTE The rise time, t_r, is the time interval between 10 % and 90 % value of 1st peak current.					

1. An equivalent model of the ESD gun is given in the model 'model_gun.sch'. Verify that the waveform complies with IEC61000-4-2. Does the first peak current change with the output load ? In the rest of the exercise, the duration of the pulse will be assumed to be equal to 100 ns.

2. We consider an application with a digital IC, whose input is connected to a long cable harness for signal transmission purpose. The signal bandwidth is equal 100 MHz. A 100 Ω termination resistor is connected at the digital input. The circuit is biased at 3.3 V. Because of the length of the cable, the digital input is exposed to ESD events. The application has to withstand the ESD Level 2 (+/- 4 kV max). The equivalent model of this input is given by the model 'model_digital_input.sym'. Its principle is described below.



C_{comp} is the equivalent input capacitance of the IC terminal. R, L, C model the input package effect. The effect of power and ground package pins is neglected. Clamp_Vdd and Clamp_Vss are the power and ground clamps respectively. They behave as diodes. The voltage applied on the pad is available on the terminal VPAD. The terminals P_W and E_uJ provide the instantaneous power (in watts) and total energy (in µJ) absorbed by each clamp. The breakdown voltage of the IC is equal to 10 V and the maximum energy that a power or ground clamp can absorb is 1.5 µJ.

a. What is the purpose of power and ground clamps ?

b. Create a new schematic with the IC input model. Connect a voltage generator Vg on the IC input. Place the SPICE command: '.DC Vg -10 10 0.1' in order to plot the static I(V) curve of the IC input. What are the voltage triggering conditions for IC internal protection clamps ? When clamps are turned on, what is their on-resistance ?

c. If we suppose that the incoming ESD is a 100 ns wide square pulse, what are the safe operation area of the static curve ?

3. The IC is now mounted on the application board and ESD pulse can be applied directly on the digital input.

a. Does the digital input withstand a direct +/- 4 kV ESD pulse ? If no, what is the more likely failure mechanism ?

b. What is the current absorbed by the activated clamp ?

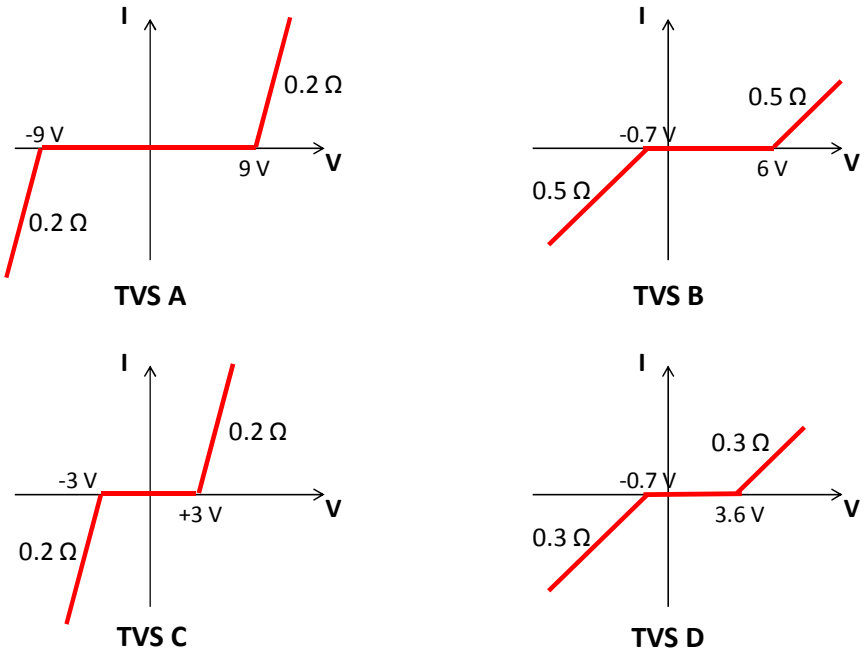
c. What is the maximum ESD level that the digital input can withstand without failure ?

4. Propose general strategies at PCB level to increase the susceptibility of the digital input to ESD pulse. Explain the purpose of the components that you propose to add.

5. Place an external series resistor before the digital input. Find the minimum resistance value to reach the +/- 4 kV susceptibility level. As the input capacitance of the IC is 10 pF, what should be the maximum resistance value to meet the bandwidth requirement ?

6. Place an external parallel capacitor before the digital input. This capacitor is supposed ideal (no parasitic effect). Find the minimum capacitance value to reach the +/- 4 kV susceptibility level. Is it acceptable to meet the bandwidth requirement ?

7. As last solution, we propose to place an external Zener-based Transient Voltage Suppressor (TVS). Four models are available, with the static I(V) curves given by the figure below. All these diodes support a maximum pulse current of 20 A.



a. Without any simulations, what should be the adequate choice(s) to protect the IC against ESD ?

b. Electrical equivalent models of the four TVS types are given in the file 'TVS_Zener_A.sym', 'TVS_Zener_B.sym', 'TVS_Zener_C.sym' and 'TVS_Zener_D.sym'. Test the protection provided by each TVS type in simulation. Which TVS devices may protect the IC input ?

c. Between the external TVS and the internal ESD clamps, what is the primary protection ?

d. The TVS is connected to signal and ground PCB traces by 5 mm trace. If we suppose that a PCB trace introduces 0.5 nH/mm, what is the effect on the voltage applied on the digital input pad ? Propose a recommendation for TVS placement.

8. Is it possible to combine protection resistor, capacitor and TVS ? Propose a general electrical schematic to protect IC input-output terminals against ESD.