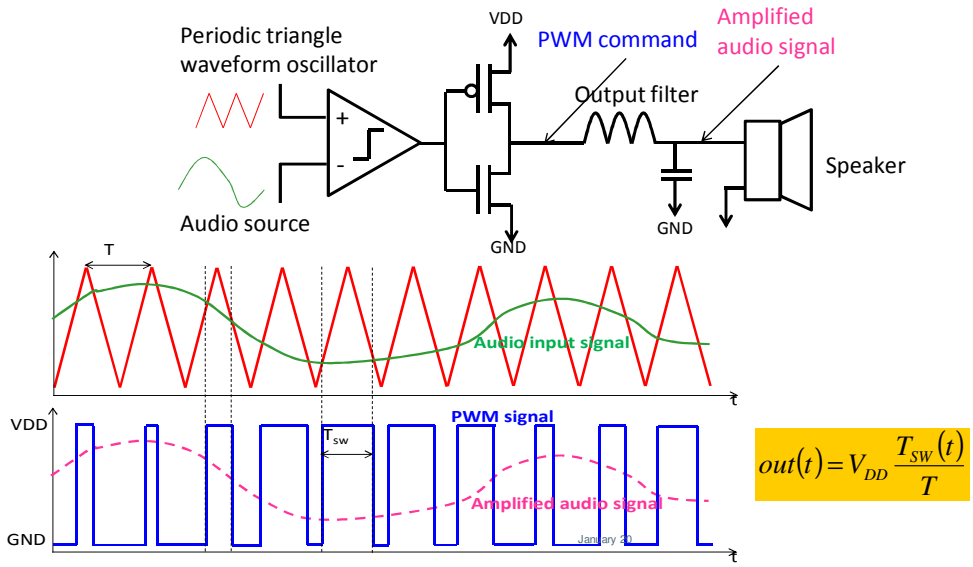
EMC Problem
Reducing emission from a class-D amplifier

This problem is focused on the basic techniques to reduce conducted emission produced by power switching devices (e.g. switched-mode power supply, power driver, switching amplifier, line driver, …). Due to the high current amplitude and fast switching rate, if they drive load connected to long cables, they can also produced intolerable radiated emission. In this problem, we consider a class D amplifier (switching amplifier) made for audio application, whose principle is described below. The output filter is required to remove high frequency content of the output current that may produce intolerable electromagnetic emission.



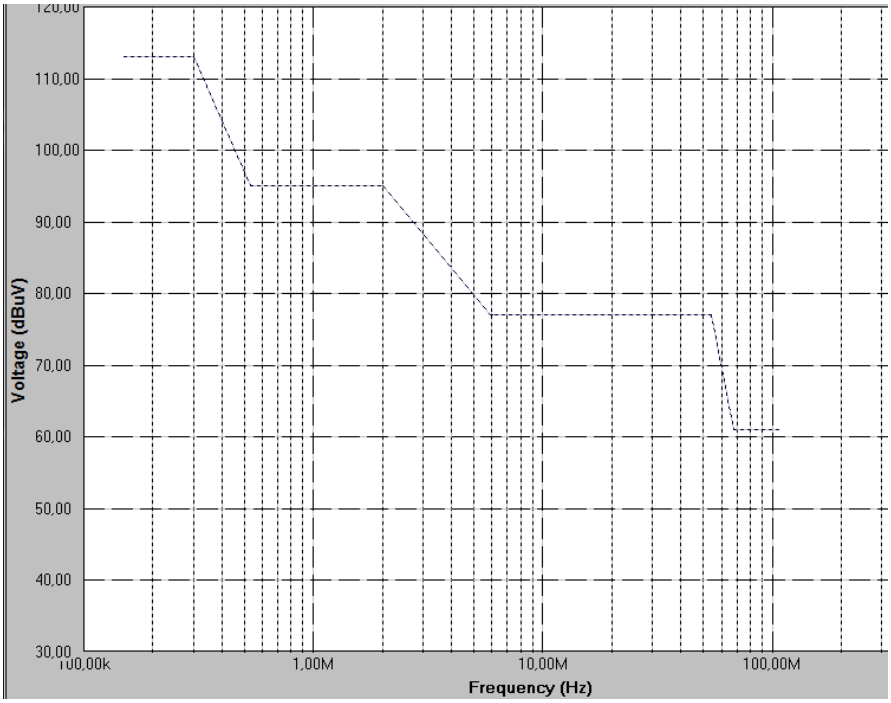
The PWM frequency is set to 200 kHz. The amplifier is designed to drive a 8 Ω speaker. In this problem, it will be modeled as a voltage generator with a 8 Ω output impedance, able to provide a maximum power of 10 W to the speaker. In its initial version, the amplifier delivers a PWM signal with rise and fall time equal to 10 ns.

The model of the speaker is given in the subcircuit 'model_speaker.sym'. The audio amplifier and the speaker are supposed to be connected by a 2-wire cable with the following dimensions:

- wire diameter = 1 mm
- wire separation = 1 mm
- cable length = 1 m
- dielectric coating permittivity = 4

The final application must comply with several EMC requirements:

- conducted emission: the voltage measured at the output of the amplifier, terminated with typical load, must comply with the standard limit CISPR25 - class 1 shown below.
- radiated emission: the electric field produced by any equipment which embeds this component at 3 m must be less than 40 dBµV/m (limit defined by standard EN55022).



Conducted emission limit according to CISPR25 - Class 1 (voltage method)

1. With the tool 'Tools > Cable Modeling', build the model of the cable valid up to 500 MHz. Save it in a subcircuit called 'model_cable_bifilar.sym'.

2. Build the equivalent model of the amplifier, which delivers a 50 % duty cycle PWM. Connect the cable and speaker model to its output. Simulate the transient profile of the voltage and current at the cable input, with the following SPICE command: '.tran 2n 100u'. At the end of the SPICE simulation, plot the spectrum of the simulated voltage and current ? Determine the frequency range(s) with the maximum conducted emission ?

3. a. Is the product compatible with CISPR25 conducted emission limit ?

b. Is the simulated current a common-mode or a differential-mode current ? Is there any common-mode current with this model ? What must be the maximum differential-mode current to comply with the radiated emission limit given by EN55022 standard ?

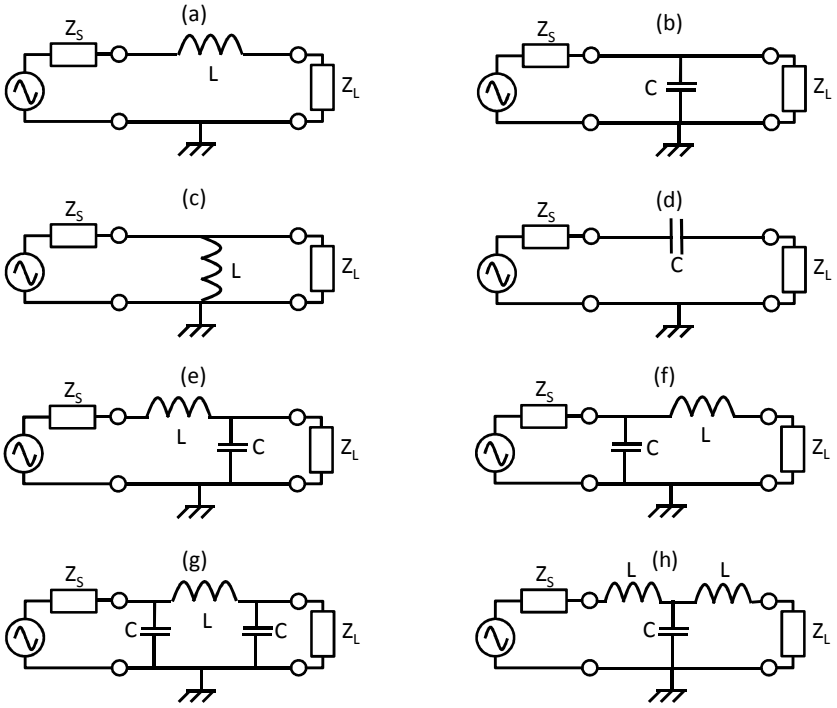
4. The amplifier circuit designer can propose buffer version with different values for the transition times, comprised between 5 ns and 200 ns, which may be compatible with power efficiency constraints.

a. Which version should you choose to reduce electromagnetic emission ?

b. What is the improvement provided by this buffer change ? Is it sufficient ? Is an EMC filter required at the output of the amplifier ?

5. In this part, we focus on the design of an EMC filter to limit the conducted emission produced by the amplifier.

a. In the following 8 filter configurations presented below, which are EMC filters ?



b. Propose a simulation test-bench with IC-EMC to simulate the insertion loss of a filter for 8 Ω source and load impedances. Find the definition of insertion loss. In IC-EMC, you can use the symbol 'Voltage ratio probe' to compute the ratio between the voltages on two different nodes. Set the following simulation command: .AC DEC 50 10k 1G.

c. Set L equal to 22 µH and C equal to 100 nF. For each EMC filter, what are the cut-off frequencies ? What are the roll-off attenuation ?

d. Test the effect of EMC filter on the conducted emission of the class D amplifier. Find the lowest order filter topology to pass CISPR25 limit.

6. Actually, passive devices used for the EMC filter are affected by stray elements:

- the inductor has a series resistance of 60 mΩ, a parallel capacitance of 20 p and a parallel resistance of 10 kΩ
- the capacitor has a series inductance of 1 nH and an series resistance of 20 mΩ

a. Simulate the actual insertion loss profile.

b. Simulate the effect on the conducted emission. What is the degradation provided by stray elements of passive devices ?

c. The mounting of each passive device add some PCB traces. We suppose that the maximum length added by passive device mounting is 5 mm and 1 mm of PCB trace introduces 1 nH. Repeat question a and b. Test the influence of capacitor and inductor mounting separately.

d. Propose a guideline for filter mounting on PCB.

7. In order to simulate common-mode radiation, the following changes are provided to the electrical model:

- the amplifier board and the cable are supposed to be placed at 50 mm above a metallic chassis structure, but they are let floating.
- there is a parasitic capacitance between the board ground plane and the chassis which is estimated to 5 pF. Its value is related to the surface of the ground plane on the PCB.
- there is a parasitic capacitance between the output node of the amplifier and the chassis which is estimated to 0.5 pF. Its value is related to the surface of the amplifier output node on the PCB.

a. With the tool 'Tools > Cable Modeling', build the model of the cable valid up to 500 MHz. Save it in a subcircuit called 'model_cable_bifilar_gnd.sym'.

b. Initially, we suppose that the transition time of the amplifier is 10 ns and no output filter have been placed. Update the electrical model to simulate the common-mode current at the cable input. The common-mode current can be extracted by adding the symbol  'Common-mode current probe' on the schematic. Launch the simulation and plot the spectrum of the common-mode current.

c. What must be the maximum common-mode current to comply with the radiated emission limit given by EN55022 standard ? Does the amplifier comply with EN55022 without output filter and transition time change ?

d. What is the effect of increase of transition time on common-mode radiation ?

e. What is the effect of the output filter on common-mode current ? Is it as efficient as differential-mode current reduction ? Why ?

f. What is the influence of the PCB surface of output node on the common-mode radiation ?