BASIS OF ELECTROMAGNETIC COMPATIBILITY OF INTEGRATED CIRCUIT

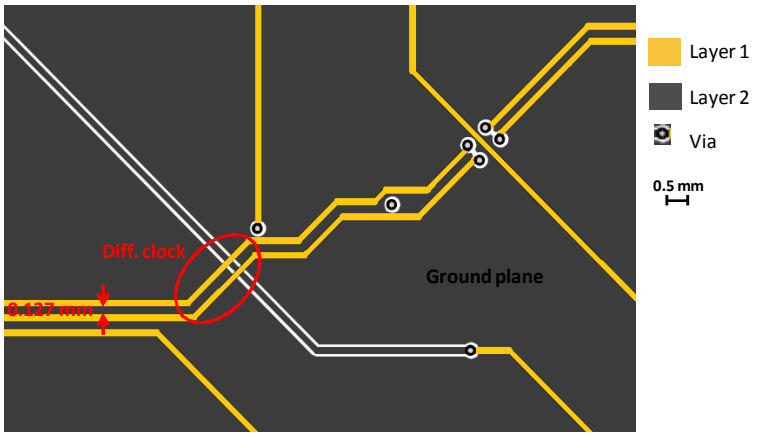
Chapter VI - MODELLING PCB INTERCONNECTS

Corrections of exercises

I. EXERCISE NO 1 - Spot the PCB design errors

Spot the six design errors in the FR4 multilayer PCB routing shown below. Indicate the error number on the PCB routing picture and precise their consequences. The characteristics of the PCB are:

- two layers are shown: layer 1 and layer 2; they are separated by 0.36 mm
- Copper traces are 0.127 mm wide and 35 µm thick. The minimum clearance between traces is 0.127 mm
- a high speed differential clock is transmitted by an edge-coupled microstrip line routed in layer 1
- the layer 2 is dedicated to a ground plane routing
- differential transmitter and receiver are 100 Ω matched
- the other traces visible on layers 1 and 2 transmit low-frequency analog or digital signals



Corrections:

The figure below shows the six errors in the PCB routing. They concern the routing of the differential clock lines, which carry a high frequency signal. The design has to be carefully done to control the line impedance and ensure symmetry to prevent differential-mode (DM) to common-mode (CM) conversion.

In the following tables, the nature and the consequences of each error are described.

Error number	Nature and consequences
1	Layer 2 serves as reference plane for the differential clock signal. It is advised to avoid any aperture in this plane close to the clock lines. Here, a trace is routed in layer 2 just below the differential clock, which leads to an impedance mismatch of the clock differential lines. Moreover, the aperture in the ground plane may radiate.
2	A via is routed very close to one line of the differential clock. Firstly, the proximity of trace and via may lead to a parasitic coupling due to crosstalk. Secondly, as the coupling between the via and both traces of the differential clock is not symmetrical,CM current is induced on the differential clock which may lead to CM emission issues.
3	According to the dimensions of the clock traces (trace width = 0.127 mm, separation = 0.127 mm, distance to the ground plane = 0.36 mm), the odd impedance of the line is nearly 45 Ω, so the differential impedance of the clock line is 90 Ω (see equation 6-15). The geometry of the clock traces (width and separation) should be changed to ensure a differential impedance closer to 100 Ω.
4	A trace is routed in very close proximity to one line of the differential clock. same consequences than error 2.
5	A via is placed between both traces of the differential clock. As the separation between both traces widens locally, an impedance mismatch is created. Moreover, one trace becomes larger than the other, leading to DM to CM conversion.
6	The designer decided to change the routing layer of the high-speed clock because a trace supporting a low-frequency signal crosses it. The series via introduces additional resistance to the clock and degrades the impedance matching. It would be better to route the differential clock on one layer and change the routing layer of the low frequency trace, whose signal integrity is less critical.

In order to limit the radiated emission, the differential clock signal should be routed in a burried layer of the multilayer PCB.

II. EXERCISE NO 2 - Modelling a differential line

A 5-cm-long edge-coupled microstrip line is designed on an FR4 substrate. The traces are made of copper 35 µm thick and 0.35 mm wide. They are separated by a distance of 0.15 mm and placed 0.2 mm above a ground plane. The losses are neglected in this exercise.

1. With the Interconnect Parameters interface, compute the per-unit-length electrical parameters of the lines (remember that line losses can be neglected in this exercise). Determine the differential- and common-mode impedances.

2. Propose two possible matching networks for this line.

3. Construct an equivalent electrical model of this line valid up to 5 GHz.

4. Place the termination network proposed in question 2 at the end of the line. Verify the correct matching of the line by S_{11} parameter simulation for the two excitation configurations: differential-mode and common-mode excitation.

5. Design a differential line for a PCB. The line is driven by a driver with a 100 Ω output differential impedance. The distance to the receiver is 7 cm. The PCB material is FR4, the minimum width and separation are equal to 0.15 mm. The height to the reference ground plane is 0.2 mm. The frequency content of the transmitted signal is assumed not to exceed 5 GHz.

a. Propose geometrical dimensions for the traces.

b. Propose a termination network for the differential line.

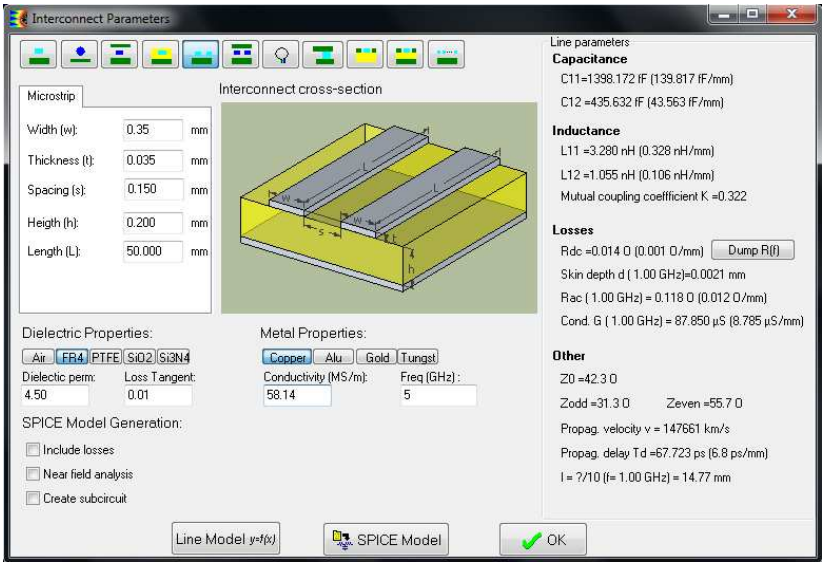
c. Build an equivalent electrical model of the differential line and its termination network. Verify the impedance matching of the line.

Corrections:

1. According to the IC-EMC "Interconnect Parameter" tool, the following values for the pul self and coupling inductances and capacitances are: l11 = 0.328 nH/mm, l12 = 0.106 nH/mm, c11 = 0.14 pF/mm, c12 = 0.044 pF/mm.

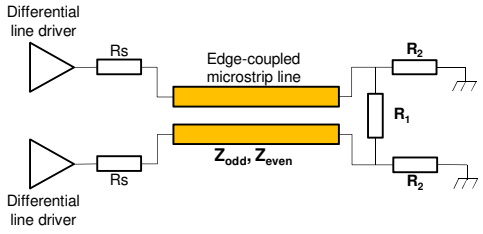
Odd and even mode characteristic impedances can be deduced (equations 6-14 and 6-13): Zodd = 31.3 Ω and Zeven = 55.7 Ω.

The differential and common-mode impedances can be deduced from the odd and even mode characteristic impedances (equations 6-15 and 6-16): ZDiff = 62.6 Ω and ZComm = 27.8 Ω.



2. According to Fig. 6-10, two matching network can be proposed:

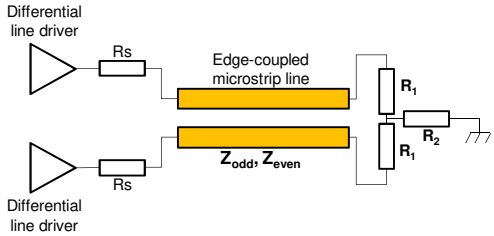
<u>Π-network</u>



$$R_1 = \frac{2Z_{even}Z_{odd}}{Z_{even} - Z_{odd}} = 143\Omega$$

$$R_2 = Z_{even} = 56\Omega$$

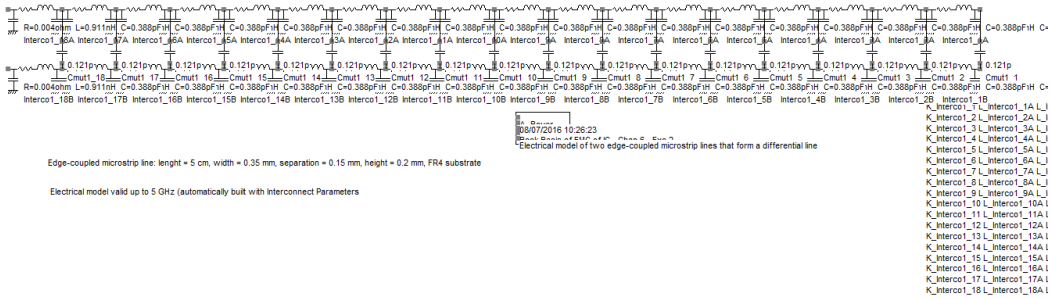
<u>T-network</u>



$$R_1 = Z_{odd} = 31\Omega$$

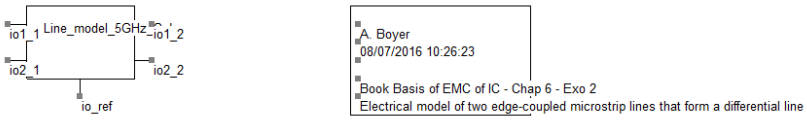
$$R_2 = \frac{1}{2}\left(Z_{even} - Z_{odd}\right) = 12\Omega$$

3. In "Interconnect Parameters" interface, type '5' in the field 'Freq (GHz)' and click on the button 'SPICE model' to generate the electrical model of the line automatically. The generated model is given in the file "Line_model_5GHz.sch". It is shown below. The model includes 36 RLC cells and 18 mutual inductors and capacitors.



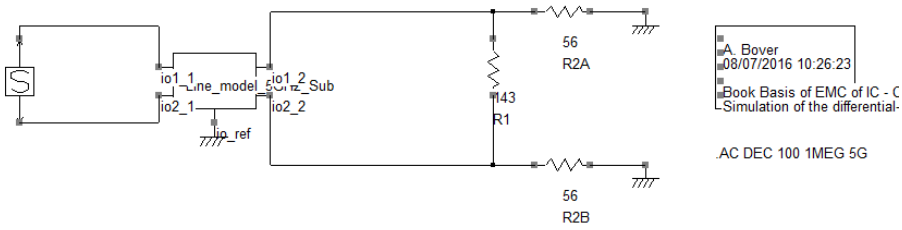
Although the equivalent electrical elements of the model are explicit, the large number of components makes difficult the reading of the model. To create more practical schematic diagram, it is recommended to save such models in subcircuit file (.sym). In "Interconnect Parameters" interface, fill the option Create subcircuit, give a file name (Line_model_5GHz_Sub.sym) in "Save subcircuit as" field and click on the button "SPICE model" and the button OK to close the interface. The subcircuit can be imported with menu command "Insert / Insert symbol (.SYM).

The file Line_model_5GHz_Sub.sch is similar to Line_model_5GHz.sch, except the model of the line is given by the subcircuit file Line_model_5GHz_Sub.sym. The model is shown below.



4. We consider only the Π-type termination network, which is placed at the output terminals of the line. The proposed models can be transformed by replacing the Π-type network by the T-type network.

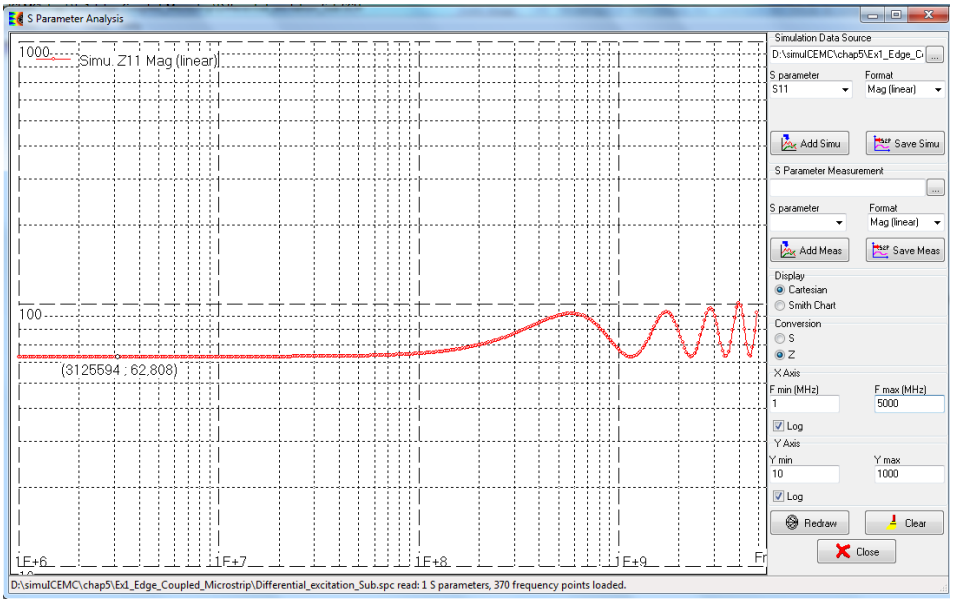
Differential-mode excitation: the excitation (a S parameter probe) is placed between the input terminals of the line to excite only the differential-mode. Open the file Differential_excitation_Sub.sch, launch a SPICE simulation and open the 'S parameter vs Freq' window to plot the impedance Z11. The impedance is nearly constant up to 2 GHz and is around 63 Ω, the differential-mode impedance of the line. Thus, the termination Π-type termination network sets the correct differential-mode impedance.



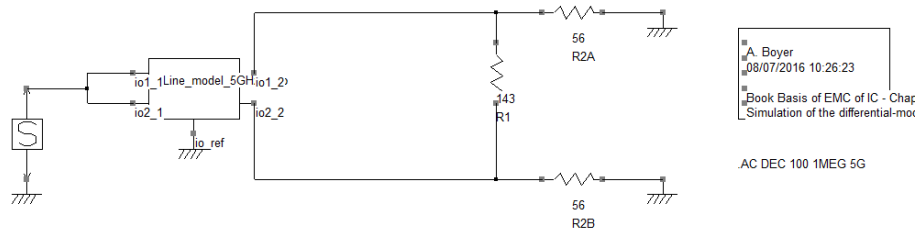
Edge-coupled microstrip line: lenght = 5 cm, width = 0.35 mm, separation = 0.15 mm, height = 0.2 mm, FR4 substrate

A pi-type matching network is placed at the output of the line

A S parameter probe is placed between the input terminals of the line to excite only the differential mode.



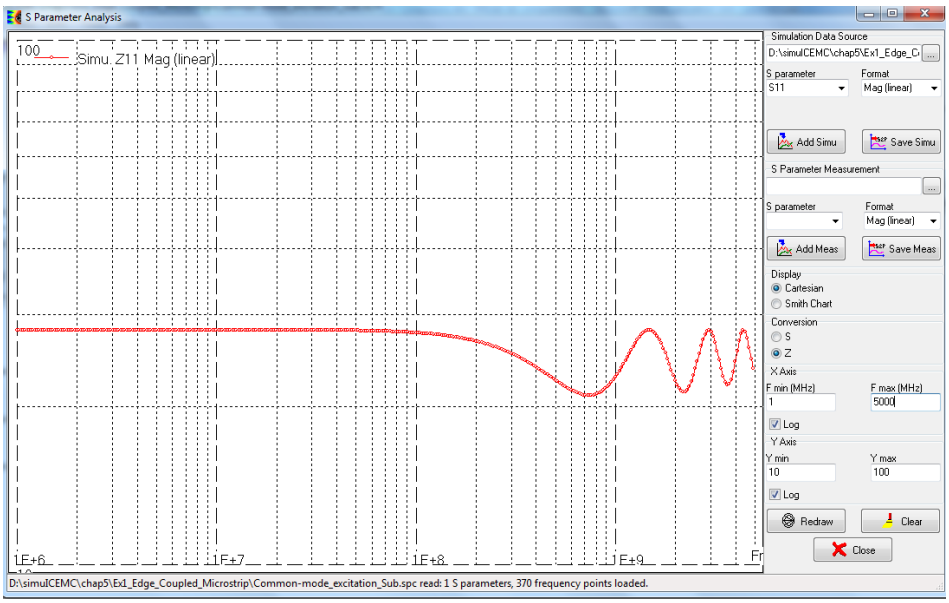
Common-mode excitation: the input terminals of the line are shorted and connected to the excitation (a S parameter probe), which excites only the common-mode. Open the file Common-mode_excitation_Sub.sch, launch a SPICE simulation ▶ and open the 'S parameter vs Freq' window ⊛ to plot the impedance Z11. The impedance is nearly constant up to 2 GHz and is around 28 Ω, the common-mode impedance of the line. Thus, the termination Π-type termination network sets the correct common-mode impedance.



Edge-coupled microstrip line: lenght = 5 cm, width = 0.35 mm, separation = 0.15 mm, height = 0.2 mm, FR4 substrate

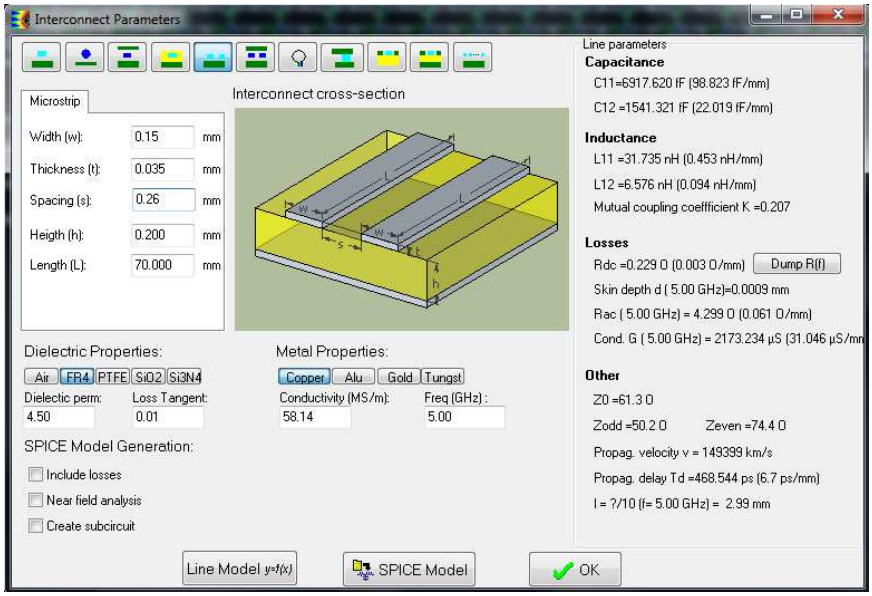
A pi-type matching network is placed at the output of the line

The inputs terminals of the line are shorted and connected to a S parameter probe is placed between the input terminals to excite only the common-mode.



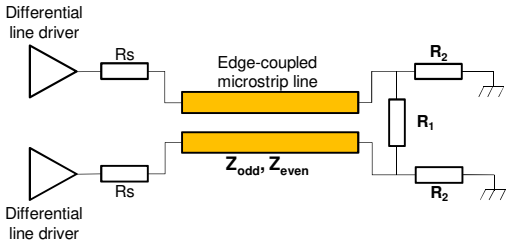
5. a. The differential impedance of the line has to be equal to the differential impedance of the driver to ensure signal integrity.

With IC-EMC, change the width and the separation of the traces until the odd-mode impedance Zodd is equal to $1/2*Z_{Diff}$ = 50 Ω. Width and separation must be larger or equal to 0.15 mm. It is better to limit the separation to make the line as compact as possible. With minimum separation (0.15 mm), no valid width can be found. We choose a width equal to 0.15 mm and a separation equal to 0.26 mm.



5. b. According to Fig. 6-10, two matching network can be proposed:

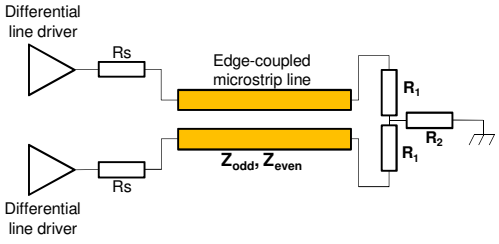
Π-network



$$R_1 = \frac{2Z_{even}Z_{odd}}{Z_{even} - Z_{odd}} = 309\Omega$$

$$R_2 = Z_{even} = 74\Omega$$

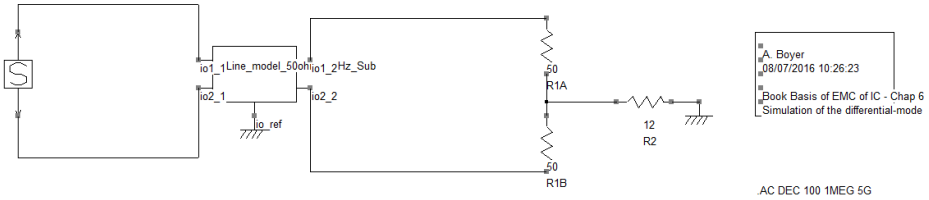
T-network



$$R_1 = Z_{odd} = 50\Omega$$

$$R_2 = \frac{1}{2}\left(Z_{even} - Z_{odd}\right) = 12\Omega$$

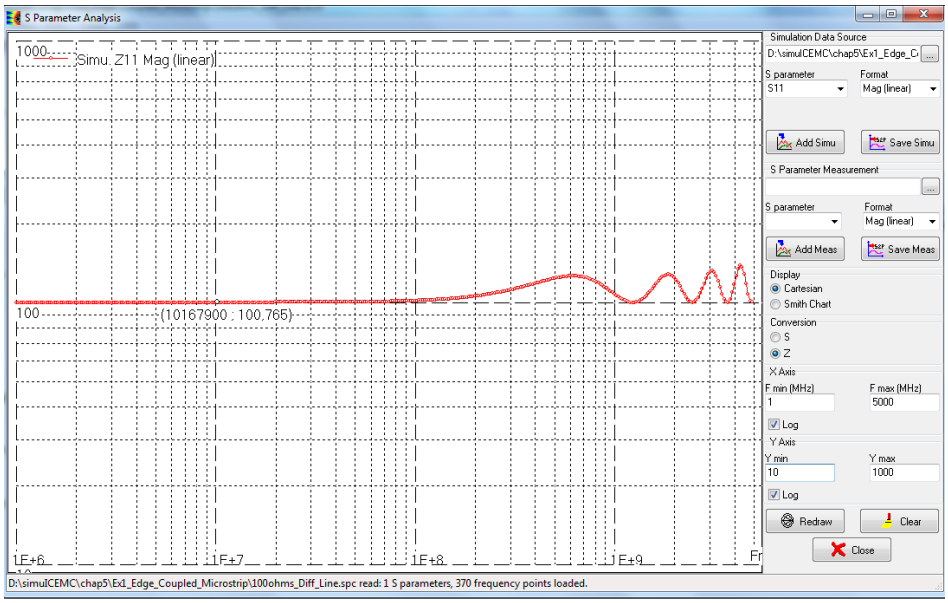
5. c. We have to verify that the differential-mode impedance of the line terminated by the Π-type or the T-type network is equal to 100 Ω. Open the file 100ohms_Diff_Line_Sub.sch, launch a SPICE simulation ▶ and open the 'S parameter vs Freq' window ⊛ to plot the impedance Z11. The impedance is nearly constant up to 2 GHz and is around 100 Ω, the differential-mode impedance of the line. The line is corrrectly matched to 100 Ω.



Edge-coupled microstrip line: lenght = 7 cm, width = 0.24 mm, separation = 0.15 mm, height = 0.2 mm, FR4 substrate

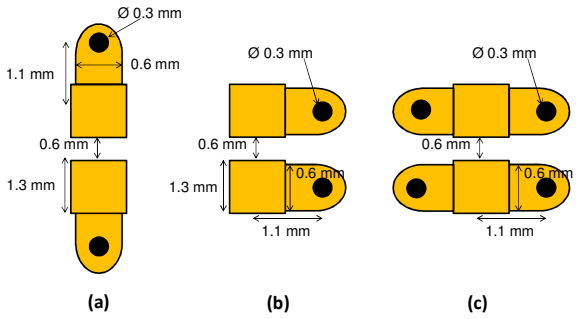
A pi-type matching network is placed at the output of the line

A S parameter probe is placed between the input terminals of the line to excite only the differential mode.



III. EXERCISE NO 3 - Mounting a decoupling capacitor on a PCB

The figure below describes three different methods for mounting a decoupling capacitor on a multilayer PCB board and connecting it to the inner power and ground planes. The dimensions of the connection traces and soldering lands are detailed. The via has a radius of 0.15 mm. The ground or power planes are considered to be 0.38 mm below the PCB surface. The PCB is 1.6 mm thick.



1. Compare the three capacitor mounting configurations. Which one is the best? Which one is the worst?

2. For each configuration, compute the parasitic inductance associated with the connection of the capacitor to the power and ground planes.

3. Let us consider the placement of a 22 nF SMT capacitor mounted in a 0805 package. The capacitor's impedance profile in the frequency domain is provided in file C22n.s1p by the device manufacturer. Propose an electrical model of the capacitor. What are the capacitor's ESL and self-resonant frequency?

4 What is the self-resonant frequency of the capacitor mounted according to the previous three configurations?

Corrections:

1. In this exercise, we want to analyze the effect of placement of via to connect decoupling capacitors to inner power and ground planes. Interconnects introduce parasitic serial inductance that degrades the decoupling performances (reduction of the self-resonant frequency, increase of impedance above the self-resonant frequency). The best configuration is the one which minimizes the parasitic inductance. Inductance is minimized when:

- the via are placed closed to the capacitor, so that the length of the trace between a via and a capacitor terminal is reduced
- the via are placed closed together. The mutual inductance between both via is increased. Thus, the total inductance of the loop forming by the capacitor, the via, the power and ground planes is minimized
- several via are connected together. Placing several inductances in parallel divides the total inductance.

Configuration (c) is certainly the best because four via are used instead of two. Reducing the separation between via would reduce further the parasitic inductance. Configuration (b) may have similar performances than configuration (c) but it is better than configuration (a) since the via are more closely spaced.

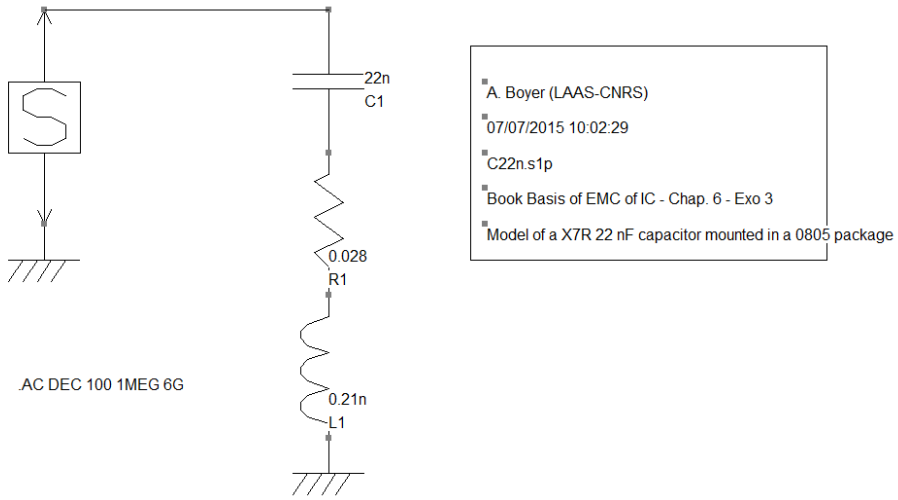
2. The procedure applied in part 4 is reused to evaluate the parasitic inductance of the capacitor mounting interconnects. Traces are assumed to be microstrip line, equation 6-11 is used to compute the parasitic inductance. Via inductance is computed according to equation 6-31. Mutual inductance between two via is given by equation 6-36. IC-EMC "Interconnect Parameters" can be used to compute the parasitic inductance associated to microstrip and via. Although this approach is not as accurate as a full-wave electromagnetic simulation, it is extremelly simple and rapid.

Configuration (a): this configuration has been addressed in part 4. The inductance introduced by a trace is Ltr = 0.25 nH. The inductance associated to a via is Lvia = 0.54 nH. The separation between both via is 3.45 mm, so the mutual inductance between both via is Mvia = 38 pH. The additional inductance due to via and trace is: Ltot = 2*Ltr+2*Lvia-2*Mvia = 1.5 nH.

Configuration (b): the inductance introduced by a trace is also Ltr = 0.25 nH. The inductance associated to a via is also Lvia = 0.54 nH. The separation between both via is reduced in this configuration: 1.9 mm, so the mutual inductance between both via is Mvia = 67 pH. The additional inductance due to via and trace is: Ltot = 2*Ltr+2*Lvia-2*Mvia = 1.4 nH.

Configuration (b): the inductance introduced by a trace is also Ltr = 0.25 nH. The inductance associated to a via is also Lvia = 0.54 nH. The separation between both via in this configuration is 1.9 mm, so the mutual inductance between both via is Mvia = 67 pH. The additional inductance due to via and trace is: Ltot = 0.5*(2*Ltr+2*Lvia)-2*Mvia = 0.7 nH.

3. The following model is proposed (Capa_22n.sch). The parasitic serial inductance of the capacitor is 0.21 nH. The self-resonant frequency of the capacitor is equal to 74 MHz.



4. Configuration (a): the total parasitic inductance is 1.71 nH, the self-resonant frequency of the capacitor is 26 MHz. The mounting configuration has seriously degraded the performance of the decoupling capacitor.

Configuration (b): the total parasitic inductance is 1.61 nH, the self-resonant frequency of the capacitor is 27 MHz. This mounting configuration provides a slight improvement of the decoupling performance.

Configuration (c): the total parasitic inductance is 0.91 nH, the self-resonant frequency of the capacitor is 36 MHz. This mounting configuration provides a significant improvement of the decoupling performance.

IV. EXERCISE NO 4 - Filtering a digital line by chip ferrite beads

A high-speed digital driver is connected to a 15 pF equivalent load through a 100-mm-long 100 Ω microstrip line designed on an FR4 PCB. The microstrip line is routed 0.38 mm from a ground plane. The transition times of the signal delivered to the load must be less than 3 ns.

This line is suspected of producing excessive radiation due to the high-frequency content of the current circulating along the line. At one metre, the electric field produced by the microstrip line must not exceed 40 dBµV/m. In order to limit its radiation, a filter may be placed at the line input. The objective of this exercise is to select a filter which reduces radiation to a minimum without significantly degrading signal integrity. The filter is selected following a simulation.

In this exercise, the driver is modelled by a square waveform voltage generator with a 33 Ω series resistance. Characteristics of the equivalent voltage generator:

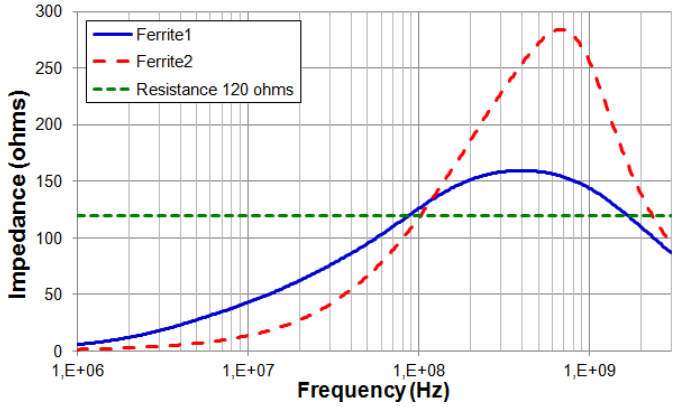
- Low/High voltage = 0 / 3.3 V
- Period = 50 ns
- Duty cycle = 50 %
- Rise/Fall time = 1 ns

1. How wide should the microstrip line be? Build an electrical model valid up to 5 GHz which includes dielectric and conductor losses.

2. Add the models of the driver and the terminal load to the microstrip line model. Simulate the voltage waveform across the load. Measure the rise and fall times as well as the positive and negative overshoot amplitude. Draw conclusions about signal integrity.

3. Simulate the current at the line input and plot its frequency content. Use equation 4-23 to estimate the worst-case radiated emission produced by the microstrip line at a distance of one metre at the following frequencies: 20, 60, 140, 180, 220, 260 and 300 MHz. Is it satisfactory?

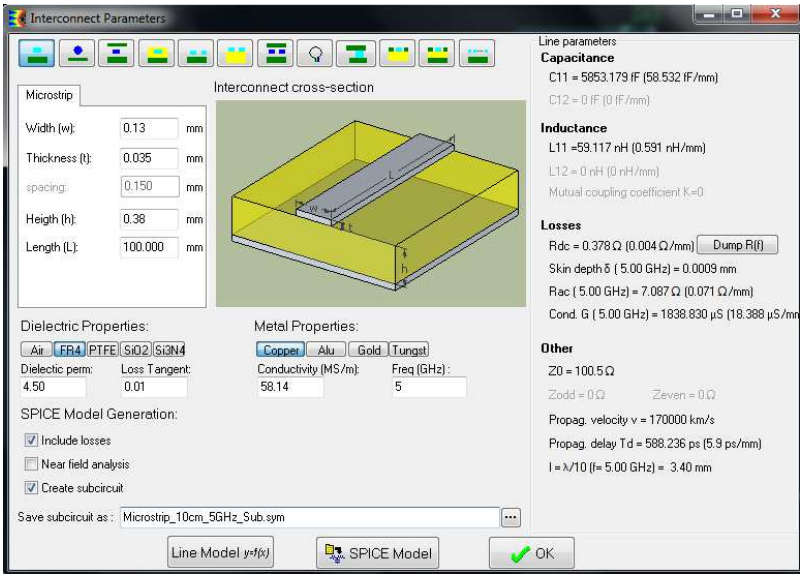
4. In order to improve signal integrity and reduce radiated emission, three filters are suggested: a 120 Ω resistor and two ferrite beads with 120 Ω at 100 MHz. The ferrite bead models are called Ferrite1 and Ferrite2. The impedance of the three filters are plotted in the graph below. The models of the ferrite beads are given in files book/ch6/Ferrite1.sch and book/ch6/Ferrite2.sch. Without performing any simulations, which would be the best filter ?



5. Build the models of the microstrip line terminated by the driver, the load and the three filter types. For each type of filter, repeat questions 2 and 3. Compare the effects of each filter on signal integrity and radiated emission. Do the results confirm your answer to question 4?

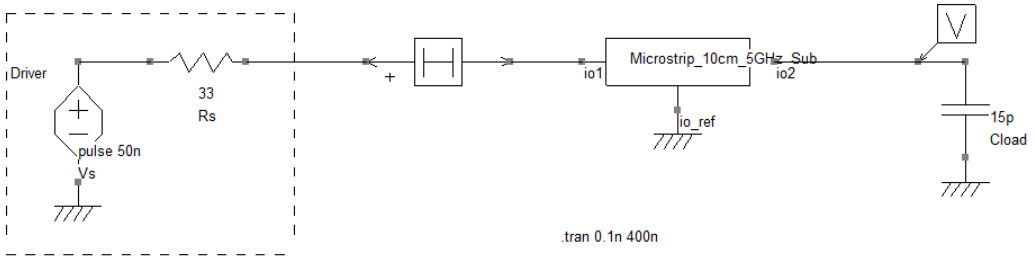
Corrections:

1. The microstrip line must have a characteristic impedance of 100 Ω. According to the PCB material characteristic and the distance to the ground plane, the width must be equal to 0.13 mm.



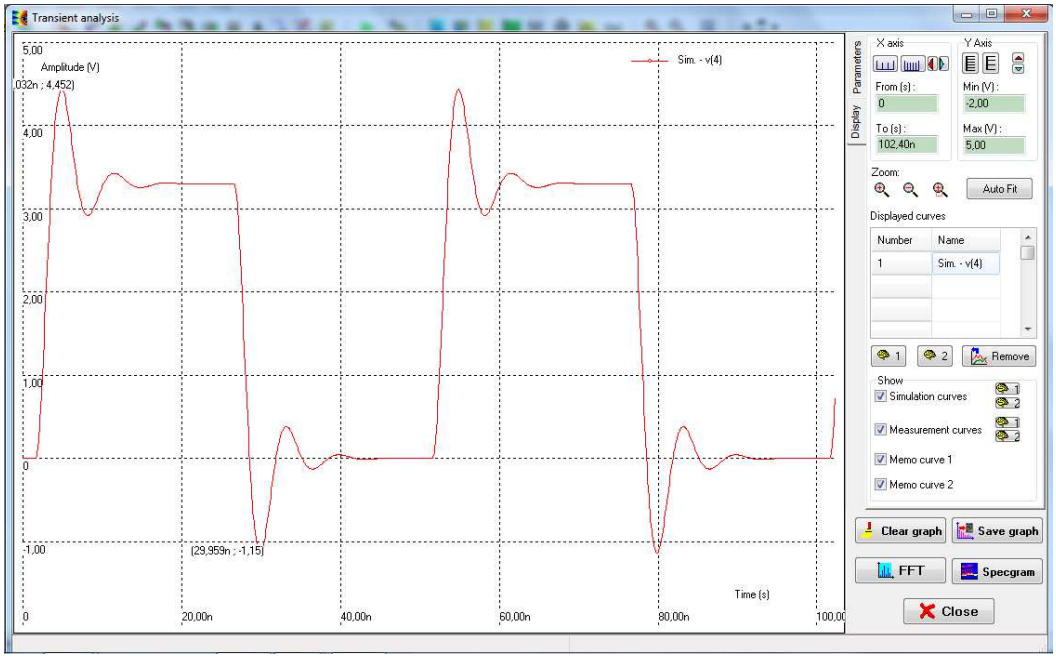
Type '5' in the field 'Freq (GHz), check the box 'Include losses'. Fill the option Create subcircuit, give a file name (Microstrip_10cm-5GHz_Sub.sym) in "Save subcircuit as" field and click on the button "SPICE model" and the button OK to close the interface. The subcircuit can be imported with menu command "Insert / Insert symbol (.SYM).

2. The model is given in the file microstrip_model_sub.sch and is shown below. The model includes the subcircuit of the lossy microstrip line, a model of the line driver and the 15 pF load. A transient simulation is configured, by clicking on "Insert / Insert analysis line".



Click on the button ▶ to generate the netlist file (.cir) and launch the simulation (with WinSPICE or LTSPICE). At the end of the simulation, click on the button to plot the time domain profile of the voltage across the load. In the part Parameters, the quantity 'Amplitude' is selected by default. Select rise time or fall time to plot their evolution. They are equal to 1.4 ns and are in accordance with the transition time requirement. However, the overshoots are about 1.1 V, which degrade the signal integrity.

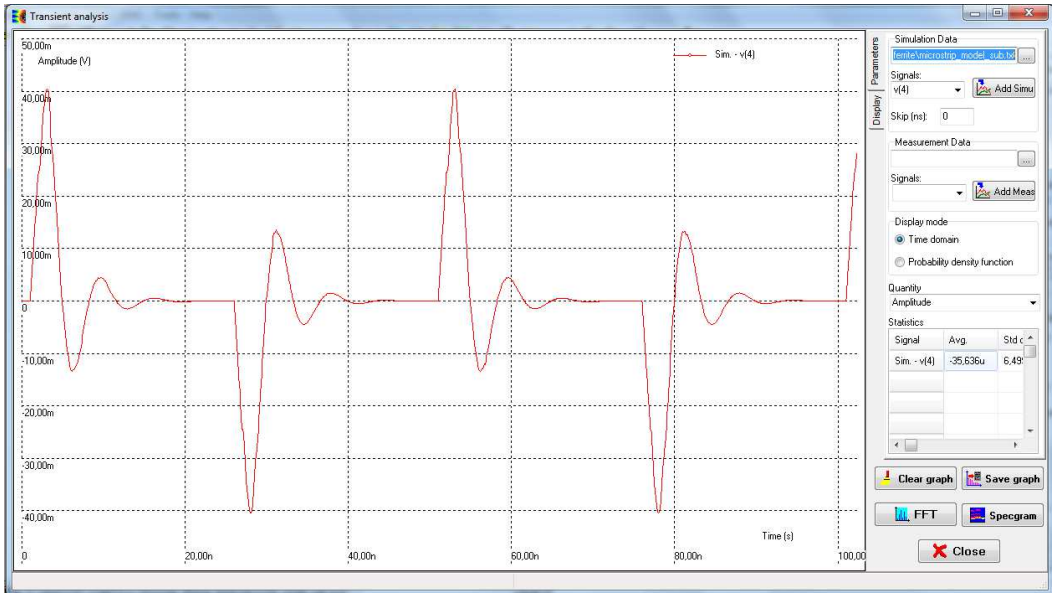
Commentaire [a1]: Bug d'IC-EMC. Il mesure 22 ns !

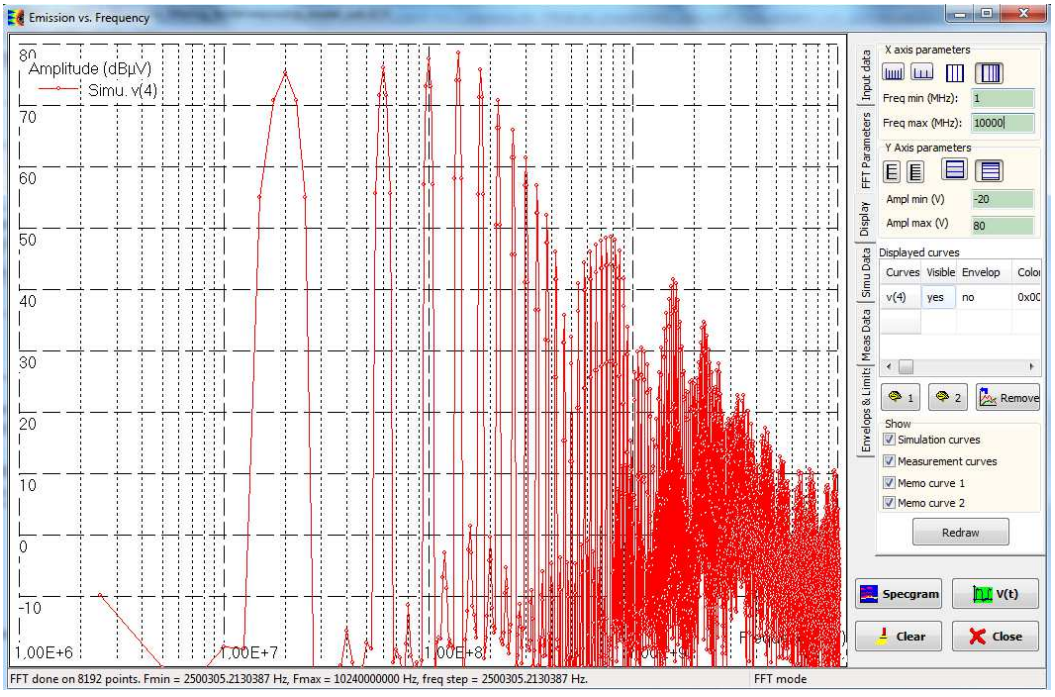


3. A current probe is placed at the input of the line. We suppose that the current amplitude is constant along the line. Click on the button and select the signal 'xx' to plot the time domain profile of the current. Click on the button FFT to plot the current spectrum.

Commentaire [a2]: Bug : le courant n'apparait pas dans la liste.

Commentaire [a3]: bug : le courant n'apparait pas. la commande de zoom axe ne marche pas.





Equation 4-23 provides simple formulations to estimate the worst case radiated emission produced by a microstrip line from its dimensions and the excitation current.

$$\begin{cases} |E_{\max}| = \dfrac{2\pi\mu_0}{c_0 r} hLf^2 I,\ L << \lambda \\ |E_{\max}| = \dfrac{2\mu_0}{r} hfI\ ,\ otherwise \end{cases}$$

where Emax is the worst case electric field measured at a distance r, h is the height of the lien to the ground plane, L is the length of the line, f is the frequency and I is the amplitude of the excitation current at frequency f. From the spectrum of the current, the worst case electric field can be estimated:

Frequency	20	60	140	180	220	260	300
Wavelength (m) (epsr = 4.5)	7.1 m	2.4 m	1 m	79 cm	64 cm	54 cm	47 cm
Current (dBµA)	75	76	78	76	71	66	61
Electric field (dBµV/m)	7	27	44	46	45	43	40

The radiated emission spectrum has a maximum at 180 MHz, and exceeds the maximum level between 100 MHz and 300 MHz.

4. The three filters will not have the same effect on signal integrity and radiated emission since their impedance profiles in frequency domain are different. Ideally, the resistance provides a constant impedance over the frequency which will reduce the current delivered by the driver. The consequences are twofold:

- the transition times are increased, so the overshoots are reduced.
- as the current circulating along the microstrip line is reduced, the radiated emission decreases

However, the resistance choice has two major drawbacks, linked to the lack of frequency selectivity of this filter:

- the filter will affect all the harmonics of the spectrum, even in low frequency. However, the transition times are mainly related to the low frequency content of the current spectrum (the first harmonics). So the increase of the transition time may become excessive and the signal integrity could be degraded.
- the resistance has to be increased to improve the radiated emission decrease at high frequency. But the transition times get longer. Thus, important reduction of radiated emission cannot be provided without degradation of the signal integrity.

Because of their frequency dependent impedance, ferrite beads offer a good compromise between signal integrity and radiated emission reduction. But the ferrite has to be chosen carefully:

- the real part of its impedance has to be large over the frequency range where the noise has to be filtered
- the real part of its impedance must not be too large at the first hamonic frequencies.

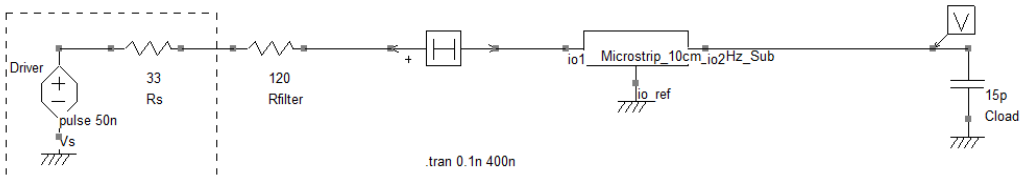
Both ferrites will be better filter than the resistance since they provide larger impedance between 100 and 300 MHz, where the radiated emission has to be reduced. Morever, their impedance is smaller at the first harmonic of the driver signal (20 and 60 MHz), so they will not increase the transition times as much as the resistor.

At first glance, Ferrite2 could be a better filter than Ferrite1 from a radiated emission since its impedance is larger between 100 MHz and 3 GHz. Moreover, as its impedance is the smallest in the 10-100 MHz range, the transition times will be less affected.

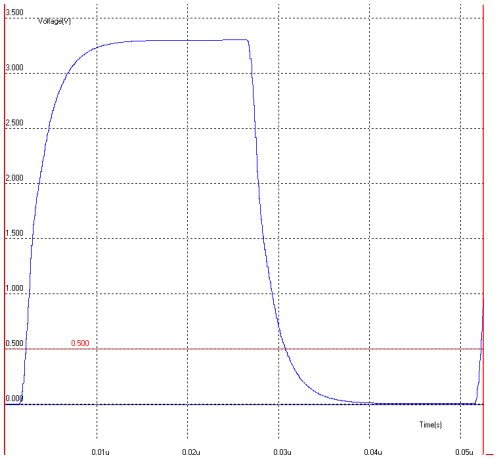
But if we analyze carefully the voltage waveform of the load voltage and the current spectrum, we observe that the main signal integrity issues are the overshoots. They are related to the 60 - 100 and 140 MHz. So Filter1 will provide a better filtering on the frequency range 60 - 100 MHz in spite of a small increase of the transition time. We can expect that Filter1 will provide a better compromize in signal integrity improvement and radiated emission reduction than Ferrite2.

In the next parts, we will verify this assumption.

5. Simulation of the effect of resistive filter (microstrip_resistive_filter.sch):

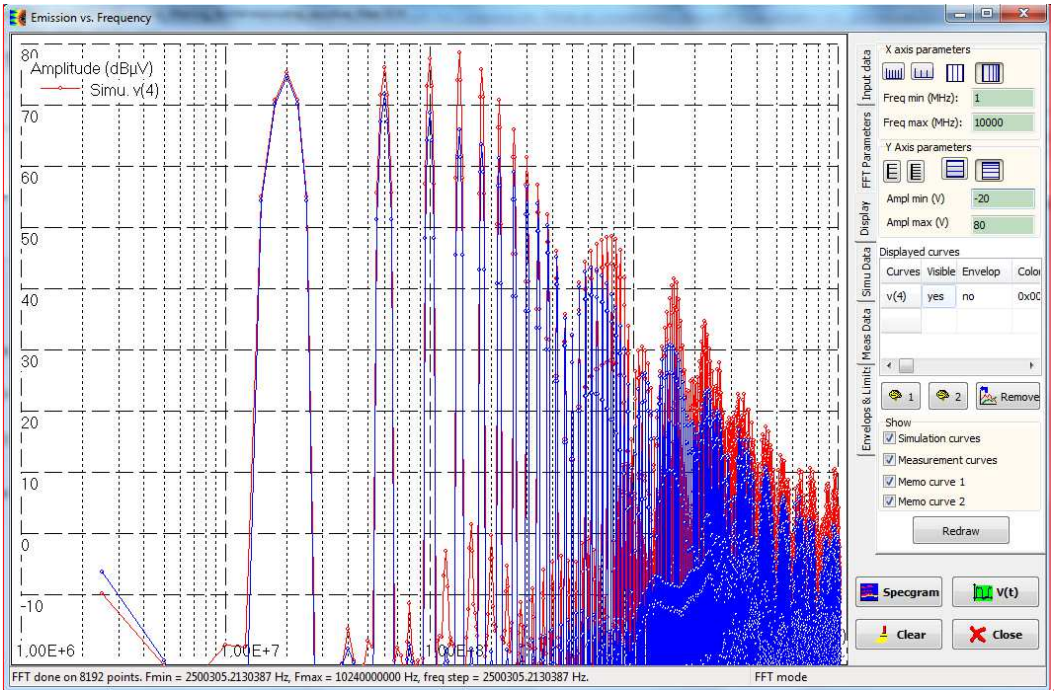


Load voltage waveform: the overshoots disappear completely, but the rise and fall times change from 1.4 ns to 4.6 ns. The transition time exceeds the 3 ns requirement.



Commentaire [a4]: A refaire

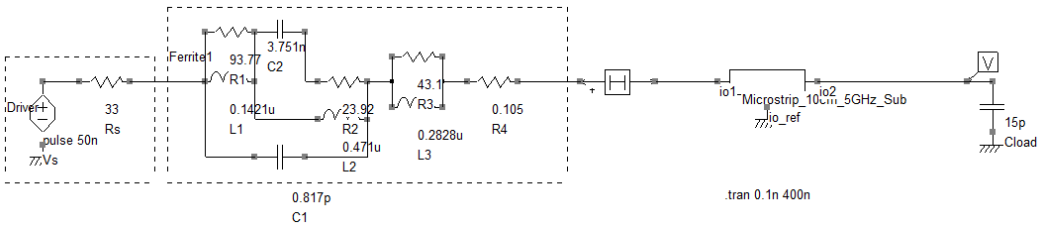
Line current spectrum (in blue = without filter, in black = with the resistive filter) and radiated emission evaluation: the resistance provides a significant radiated emission decrease between 20 and 300 MHz, and above 600 MHz. The radiated emission maximum is now 4 dB below the limit.



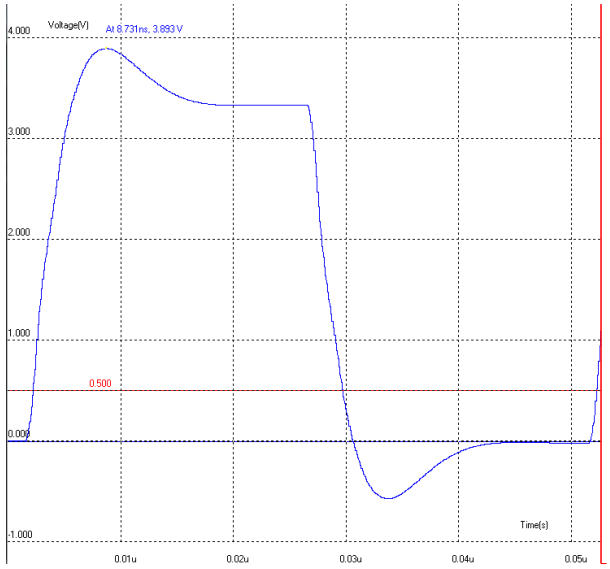
Commentaire [a5]: A refaire (la légende la courbe Memo n'apparait pas.
Bug quand on ouvre à nouveau l'écran.

Frequency	20	60	140	180	220	260	300
Wavelength (m) (epsr = 4.5)	7.1 m	2.4 m	1 m	79 cm	64 cm	54 cm	47 cm
Current (dBµA)	72.5	70	65	63.5	61.5	59	56.5
Electric field (dBµV/m)	4.5	21	31	34	35	35.5	35.5
Radiated emission improvement (dB)	-2.5	-6	-13	-12	-10	-7.5	-4.5

Simulation of the effect of ferrite bead Filter1 (microstrip_Filter1.sch):

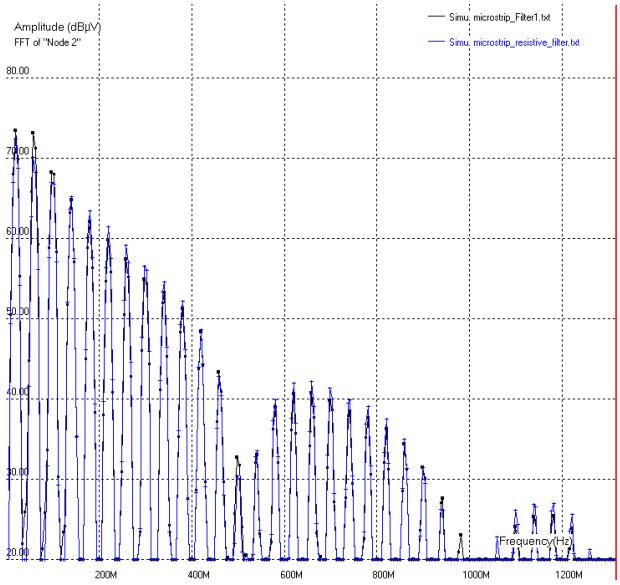


Load voltage waveform: the overshoots are damped significantly (their amplitude is equal to 0.6 V). The rise and fall times change from 1.4 ns to 2.8 ns so it complies with the 3 ns requirement.



Commentaire [a6]: A refaire

Line current spectrum (in blue = with resistive filter, in black = with ferrite bead Filter1) and radiated emission evaluation: the ferrite bead provides a significant radiated emission decrease. Compared to the resistive filter, the radiated emission decrease is improved by 1 - 2 dB between 100 and 300 MHz. The radiated emission maximum is 5.5 dB below the limit.

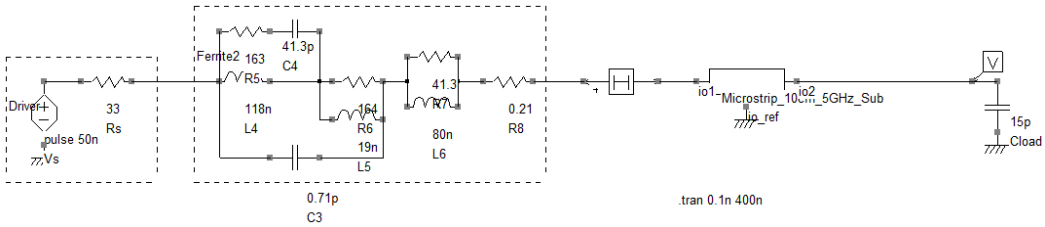


Commentaire [a7]: A refaire

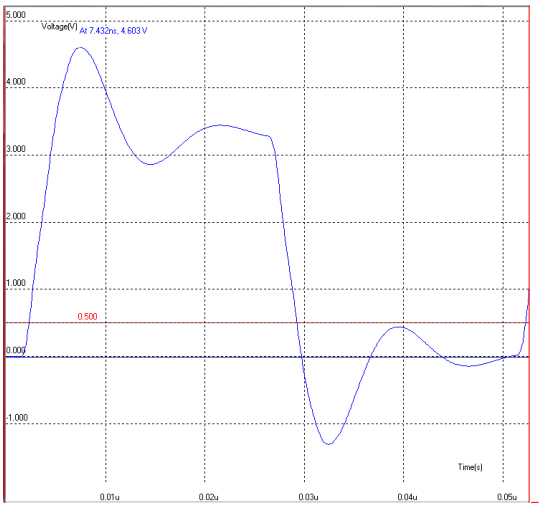
Frequency	20	60	140	180	220	260	300
Wavelength (m) (epsr = 4.5)	7.1 m	2.4 m	1 m	79 cm	64 cm	54 cm	47

							cm
Current (dBµA)	73.5	73	64.5	62	60	57.5	54.5
Electric field (dBµV/m)	5.5	24	30.5	32	34	34.5	33.5
Radiated emission improvement (dB)	-1.5	-3	-13.5	-14	-11	-8.5	-6.5

Simulation of the effect of ferrite bead Filter2 (microstrip_Filter2.sch):

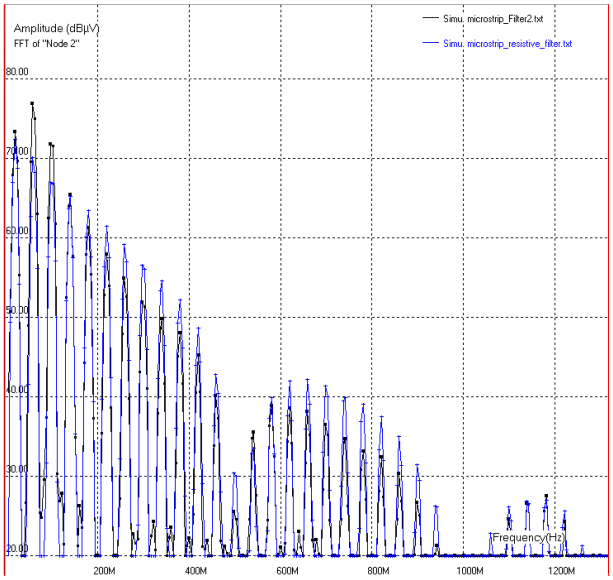


Load voltage waveform: the overshoots have not disappeared and their amplitude increases slightly (their amplitude is equal to 1.3 V). The rise and fall times increase slightly from 1.4 ns to 2.3 ns.



Commentaire [a8]: A refaire

Line current spectrum (in blue = with resistive filter, in black = with ferrite bead Filter2) and radiated emission evaluation: the ferrite bead provides a significant radiated emission decrease, except at 60 MHz. Compared to the resistive filter, the radiated emission decrease is improved by 1 - 5 dB between 100 and 300 MHz, and 1 - 3 dB compared to Filter1. The radiated emission maximum is 8 dB below the limit.



Commentaire [a9]: A refaire

Frequency	20	60	140	180	220	260	300
Wavelength (m) (epsr = 4.5)	7.1 m	2.4 m	1 m	79 cm	64 cm	54 cm	47 cm
Current (dBµA)	73.5	77	65.5	61	58	55	51.5
Electric field (dBµV/m)	5.5	28	31.5	31	32	32	30.5
Radiated emission improvement (dB)	-1.5	+1	-12.5	-15	-13	-11	-9.5

Conclusion:

The three filters reduce the radiated emission below the limit at 40 dBµV/m: Filter2 is the more efficient above 100 MHz, resistive filter is the least efficient.

However, Filter2 degrades the signal integrity: although the transition times is slightly increases, the overshoots increase. The resistive filter cancels the overshoot completely but the transition times is multiplied by 3. Filter1 provides a good compromize between transition time increase (multiplied by 2) and overshoot limitation (ony 0.6 V).

These results confirm the assumption done in question 4: the ferrite bead Filter1 is the best candidate: it improves the signal integrity (the overshoot is reduced without an excessive increase of transition times) and solves the radiated emission issue between 100 and 300 MHz.