Using ICEM Model Expert to Predict TC1796 Conducted Emission

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Abstract: This paper describes an example of the use of the ICEM model expert for comparing conducted measurements and simulations within the range 1MHz-1GHz. We consider the model of a 32-bit micro-controller based on the ICEM standard, to obtain an accurate prediction of radiated emission in TEM cell up to 1GHz, in order to forecast the impact of core noise, I/O noise and the effect of on-chip decoupling.

This work has been conducted in cooperation with T. Steinecke, Infineon (Munich, Germany), within the European Research project MESDIE.

Keywords: IC emission modeling, ICEM, ICEM model expert

Files of this case study may be found in "case_sudy/tricore"

1 Introduction

Parasitic emission caused by the switching activity of integrated circuits (ICs) has increased in importance with the tremendous progress in Complementary Metal-Oxide Semiconductor (CMOS) technology. According to the International Technology Roadmap for Semiconductors (ITRS) [1], the 22-nm CMOS process will be made available for production in 2012, featuring a standard operating frequency near 30 GHz for processing units, and the capability to integrate within a 3x3cm silicon die more than one billion transistors. When switching, each gate generates a small current pulse which flows mainly on the supply lines. The addition of these elementary current pluses provokes enormous current flows within the chip, close to 1000 A in the latest generation of high performance micro-processors.

Due to these transient currents, the ICs may generate conducted and radiated parasitic emission. The peak emission level tends to increase with the technology scale down, and may provoke severe interference inside and near the IC.

This application note describes the use the tool **ICEM Expert** of IC-EMC for the simulation of parasitic emission of integrated circuits. As an example we provide a simple circuit model of 32 bits micro-controller from Infineon [2] based on the ICEM standard [3], to obtain an accurate prediction of radiated emission in TEM cell up to 1GHz, in order to forecast the impact of core noise, I/O noise and the effect of on-chip decoupling.

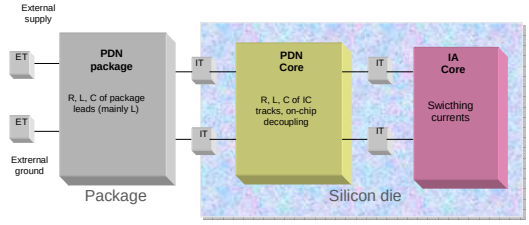


Figure 1: ICEM Model principle [3]

Figure 1 illustrates the functional principles of ICEM. Its innovation consists in the presence of active elements, which are used to represent the internal core activity of the IC, and passive elements that account for package leads and on-chip tracks.

2 Simulation flow of parasitic emission

The general flow for predicting parasitic emission is illustrated in Fig. 2. The IBIS loader gives information about the input/output characteristics, the package characteristics and supply model. The tool ICEM Model Expert is used to build the ICEM-based model of the IC by estimating the Passive Distribution Network (PDN) and Internal Activity (IA) of the IC based on general information. The IA internal core activity evaluator translates the integrated circuit specification into a current source which aims at modeling the core switching noise and on-chip decoupling. The analog simulation is performed by WinSpice and a post processing features an immediate comparison of predicted and measured spectrum in frequency domain.

The ICEM Expert tool relies on technological parameters listed in ".tec" files, adjusted for each technology node. The parameters worth of interest are:

- The typical switching current per gate
- The typical gate switching delay
- The default gate decoupling capacitance

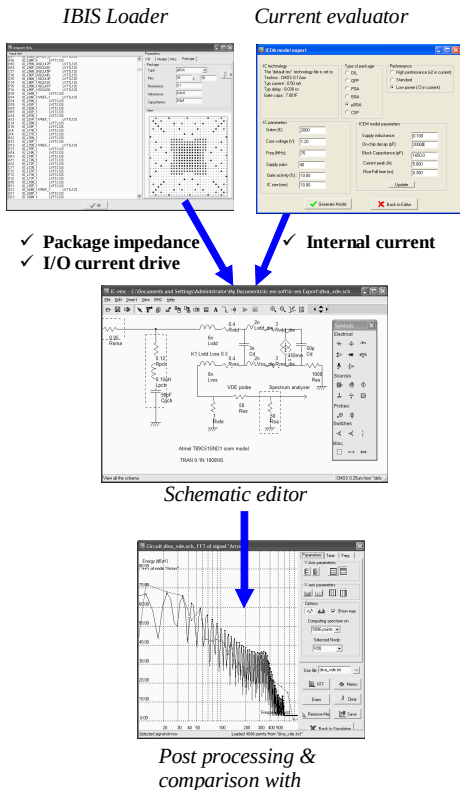


Figure 2 : Flow for simulating the parasitic emission using ICEM expert

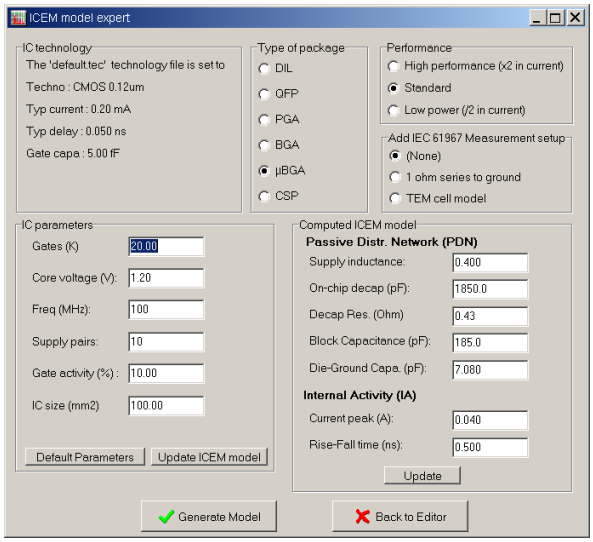


Figure 3 – The ICEM Expert menu

The “Type of package”, selects the family of package, which has a direct impact on package inductance.

The “performance” menu tunes the current peak (Ib) by increasing the peak current by 100% in “high speed” mode as compared to standard mode. In “low power” mode, the current is reduced by 50%.

Several parameters that have a direct impact on the ICEM model are given:

- The number of gates
- The core voltage
- The operating frequency
- The supply pairs
- The % of switching activity in each active edge of the clock
- The IC size in mm

The computation of the ICEM elements is performed using the following assertions (Table 1).

Ldie_vdd = sqrt(icSurface) *inductanceFactor; Rdie_vdd = sqrt(icSurface) *resistanceFactor;
imax=icPerfo*Gates*typ_current* Gate_Activity/spreadFactor;
tr := typ_Delay*SpreadFactor;
Lpack_vdd :=L_package/SupplyPairs;
Cd := Gate_Capa*Gates+ icSupplyPairs*ioCapa+ icSurface*SurfaceCapa;
Cb := Cd/10
defaultRcd = 1.0; // (Ohm) Decap_Res := defaultRcd/ln(icSupplyPairs)
Cdg:= eps0*icSurface*packEpsr /icAltitude;
CxFactor = 1fF/mm^2; Cx:= CxFactor*icSurface;

Table 1: assertions for computing ICEM parameters

- The serial inductance and resistance are proportional to the width of the die. The factors are around 0.1, if the IC size in in mm.
- The peak current of the source Ib is compute using several parameters: the spread factor is around 10; icPerfo is equal to 2 for high performance, 1 for standard and 0.5 for low power option.
- The rise and fall time of the current source is multiplied by the spread factor.
- The serial inductance is divided by the number of pairs. The inductance per pin depends on the package technology (15 nH for DIL down to 1nH for CSP).
- The decoupling capacitance is the sum of the gate capacitance, the Io capacitance and the die surface capacitance.
- The local block capacitance Cb is 10 times lower than the total capacitance
- A parasitic serial resistance is added to the decoupling capacitance to account for interconnect access to physical resistance.
- The die-to-ground capacitance is computed using a simple surface capacitance formulation, given physical parameters such as the surface of the die, the relative permittivity of the package and the IC altitude to ground.
- For TEM cell coupling, we use a value Cx which accounts for the coupling between the silicon die and the septum plate, which is the order of 1fF/mm2

The following circuits may also be added:

- A 1-Ω serial resistance on the ground path, associated with 50-Ω adaptation as defined in the IEC standard “1/150Ω conducted measurement method”. A probe is placed at the location of the measurement system, usually a spectrum analyzer.
- A capacitance/inductance coupling with the septum of the TEM cell, associated with 50-Ω terminations, as defined in IEC standard “TEM radiated measurement method”. A probe is placed at the location of the measurement system, usually a spectrum analyzer

3 Case Study

We illustrate the tool usage on the Infineon TriCore case study [2], an advanced 32-bit microcontroller dedicated to automotive applications. Simulations have been performed in advanced phase using the ICEM model expert, based only on the component data sheet information and the IBIS model provided by Infineon.

Figure 4 : The 32-bit microcontroller TriCore TC1796 from Infineon [2]

3.1 IC reconstruction from IBIS

Click “File” → “Load IBIS file” and select “infineon_tc1796_v2.ibs” in “case_study > tricore”. Click the item “Infos” to get general information about the component. Figure 5 describes the IBIS interface after opening the IBIS file and the general information of the file. Figure 6 presents 2D and 3D views of the reconstructed package from IBIS file. We notice that the component has 50 “POWER” pins, and 66 “GND” pins.

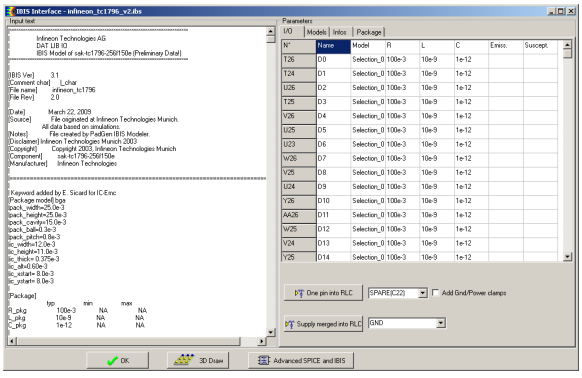
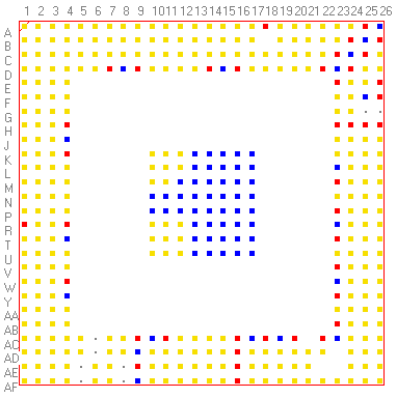
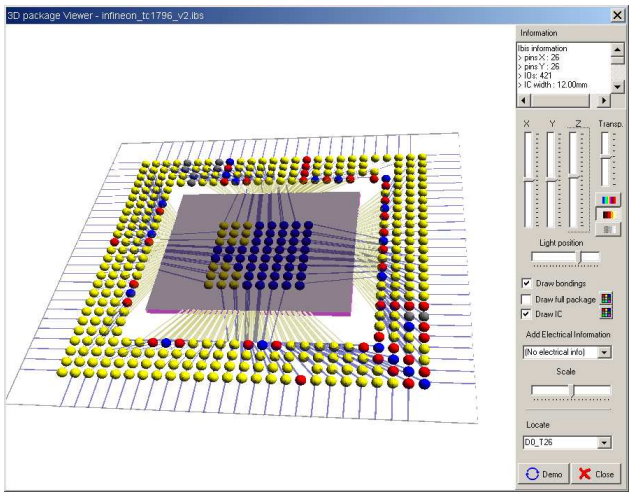


Figure 5 : Downloading the TriCore TC1796 IBIS file (infineon_tc1796_v2.ibs)



(a) 2D-view



(b) 3D-view

Figure 6 : 2D and 3D view of the TriCore TC1796 based on the IBIS file information (infineon_tc1796_v2.ibs)

3.2 ICEM Expert Parameters

Before launching ICEM Model Expert, load the technological parameters. The Tricore is designed in CMOS 0.12 µm technology. Click on File → Select technology, and open the file Lib\cmos012.tec. The parameters used to define the TriCore component in the ICEM model expert interface are listed in table 5-8. Most parameters are unconfirmed by the foundry, except the voltage supply, and number of supply pairs. Click “Generate Model” to create automatically the schematic diagram corresponding to the given parameters (Fig. 7).

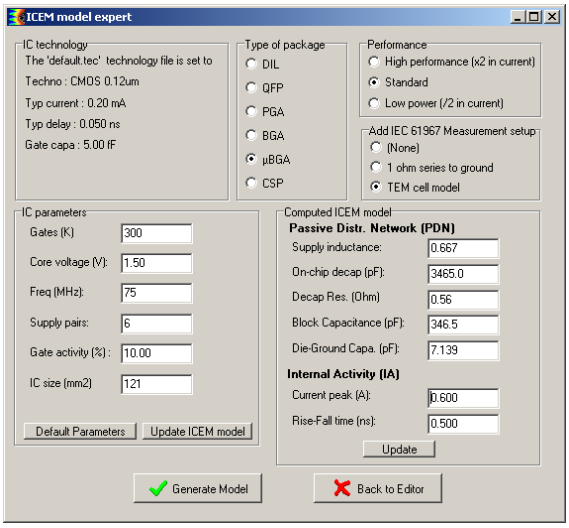


Figure 7: ICEM model expert tuned with Tricore information

Parameter	Value	Description
Technology	Cmos012 .tec	CMOS 0.12µm technology, 0.2 mA/gate peak current
Gates (K)	300	The TriCore core complexity is estimated to 300 K Gates (unconfirmed, can be tuned)
Core Voltage (V)	1.5	The logic core is supplied by 1.5V external voltage source (data-sheet)
Freq (MHz) :	150 - 75 MHz	The CPU clock of the Tricore operates at 150 MHz, with a multi-phase system (data sheet), while the peripherals and the external memory bus operates at 75 MHz
Supply pairs	58	The component has 50 “POWER” pins, and 66 “GND” pins (“Infos” in IBIS windows). We approximate to 58 pairs.
Gate activity (%)	10	At each clock edge, only 10% of the gates switch (unconfirmed, can be modified).
IC size mm^2)	69	(information from Infineon)
Type of package	µBGA	Package pitch is 0.8mm, package ball diameter is 300µm (information from data sheet)
Performance	Standard	Neither very high speed (PC, servers) nor very consumption (mobile phones).
IEC 61 967 measurement standard	TEM Cell	Measurements provided by Infineon concern TEM cell measurements

Table 2: TriCore parameters used in the ICEM model expert

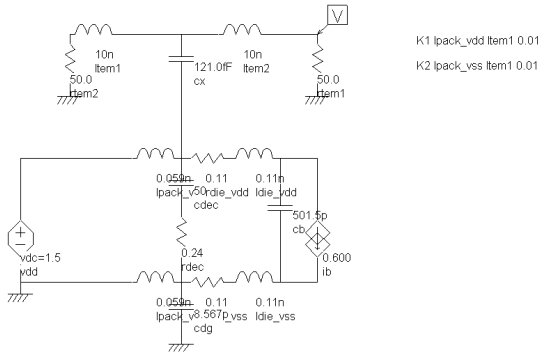


Figure 8: Schematic diagram generated by the ICEM model expert, ready for simulation (TriCore_core_tem.sch)

The default name is « example.SCH », use « File → Save As » to save the schematic diagram, for example as « TriCore_core_tem.sch ».

3.3 Comparison with TEM measurements

The IC manufacturer has published [3] TEM-cell measurements of the component, with two setups: one with core only, the second one with IOs.

Generate the SPICE file, execute the CIR file with WinSpice, and click “Emission vs. Frequency”. Click “Add Measurements” and select “TriCore_core_tem.tab” in “case_study\Tricore” . The file includes the envelop of the TEM cell measurements performed on the TriCore, core alone, without any IO activity. The comparison with measurements is given in Fig. 9. It can be seen that the noise is overestimated by the default model.

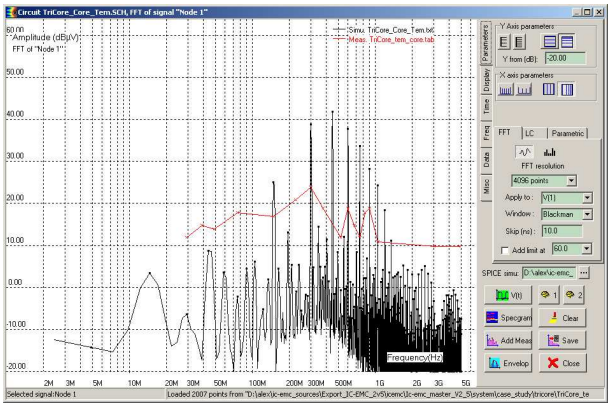


Figure 9 : Comparison between the model generated by the ICEM model expert and real-case TEM measurements (TriCore_core_tem.tab)

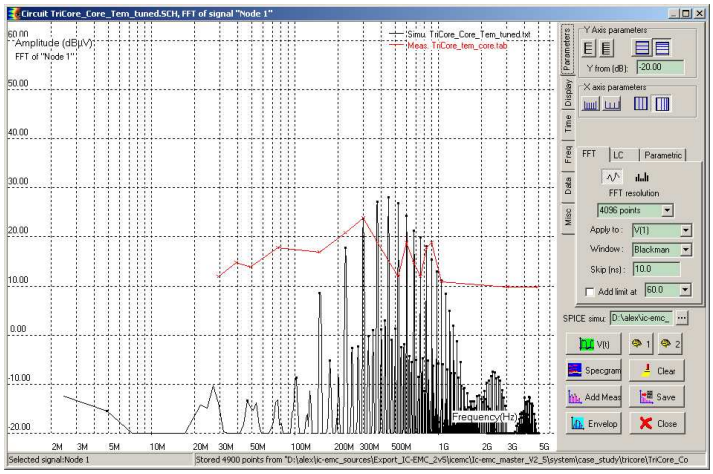


Figure 10: Comparison between the tuned model and real-case TEM measurements (TriCore_core_tem_tuned.tab)

Decrease inductive coupling	K1 Lpack_vdd Item1 0.01 L2 Lpack_vss Item1 0.01	Default value is 0.01, equal to 1% coupling. This situation corresponds to one single lead. We may use K=0.001 (coupling of 0.1%) because the supply lines are routed in all directions and do not couple strongly with the septum
Increase on-chip decoupling	Cdec → 20 nF	The EMC design experts have increased the on-chip decoupling capacitance (confirmed by Infineon) to 20 nF
Decrease peak current	Ib > I2 → 0.3 mA	The peak current might be less than expected, due to the use of low-power technology
Decrease current peak frequency to 75 MHz	Ib > Period → Increase to 13.33 ns (75 MHz)	Given a 75 MHz clock, we assume two equal current peaks, one at the rise edge, one at the fall edge, so that Ib frequency is 150 MHz. If we are in a 2-phase or 4-phase system, the main peak might appear at 75 MHz rate or even 37.5 MHz rate.

Table 3: Possible tuning of the ICEM model and associated justifications

The model needs to be tuned to match the measurements. Possible actions are listed in table 3. The new simulations performed with WinSpice on the tuned model show some reasonable correlation as shown in figure 10, even if simulations are a little higher than measurements for almost all harmonics.

References

[1] The ITRS roadmap for semiconductors may be downloaded from http://www.itrs.net

[2] "TriCore 2 - 32-bit Unified Processor Core v2.0 Architecture", Architecture Manual (PDF on line, www.infineon.com), Edition 2006, Infineon Technologies AG, D-81541 München, Germany

[3] IEC 62433-2 – ICEM : "EMC IC modeling part 2 : Models of Integrated Circuits for EMI behavioural simulation – Conducted Emission Modelling", 2008 www.iec.ch

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[5] Steinecke, T. « Experimental characterization of switching noise and signal integrity in deep submicron integrated circuits », IEEE International Symposium on Electromagnetic Compatibility, Volume : 1 , 21-25 Aug. 2000, pp 107 – 112.