S12X Case study

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Abstract: An emission and susceptibility models for a 16-bit microcontroller S12X has been constructed, and addresses the radiated emission in TEM cell, the near-field scan and the Direct Power Injection approach.

Keywords: ICEM model, conducted and radiated emission, near-field scan, susceptibility simulation

1 Introduction

The aim of this application note is to describe the full process of construction of emission and susceptibility models for a complex circuit: a MC9S12XDP512 microcontroller from Freescale, from the family S12X [1]. The radiated emission in TEM cell based on IEC 61967-2 standard as well as near-field scan emission (IEC 61967-3) are simulated and compared to measurements, within the frequency range 10 MHz to 1 GHz. A set of information related to the microcontroller model construction is given. A unique electrical model based on ICEM approach is used to predict radiated emission measured in TEM cell and near field scan [2] [3]. Direct Power Injection measurements were also performed on the S12X microcontroller and a model was produced. This case study describes the model construction and compares simulation results with measurements [4].

2 Microcontroller overview

The S12X is ideally suited for a number of automotive applications, including gateway and central body control, instrumentation, and door modules. The S12X family offers a 16-bit CPU together with a co-processor named XGATE to offload from the main CPU tasks such as basic gateway activity and peripheral-related processing. The S12X from Freescale has an internal architecture shown in figure 1. It can be noticed that the core is routed in standard cells at the left bottom part of the IC. The regulators are located in two places. A significant part of the silicon surface is dedicated to memories (RAM, Flash, EEPROM, Dual port RAM).

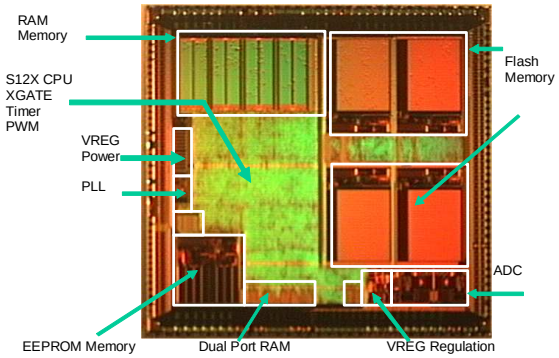


Figure 1 : S12X die structure (Courtesy Freescale SAS)

3 Ibis File Construction

An IBIS model has been constructed based on the S12X specifications ("case_study\s12x\s12x_v2.ibs"). The first step consists in defining the header of the IBIS file. The second step consists in giving typical, minimum and maximum values for the package parasitic R,L,C elements. The minimum value corresponds to the shortest package lead, the maximum value to the longest lead.

Parameter	Suggested value
[IBIS Ver]	3.1
[File name]	S12X_v2.ibs
[File Rev]	1.0
[Date]	05/03/18
[Source]	Freescale - INSA
[Notes]	information corresponds to …
[Disclaimer]	« This information is for modeling purposes only »
[Component]	Freescale MC9S12XDP512
[Manufacturer]	Freescale
[Package]	R_pkg 0.05 0.03 0.1 L_pkg 5nH 4nH 8nH C_pkg 0.5pF 0.4pF 0.8pF

Table 1 : IBIS header information

The third step consists in building the list of pins (starting [pin] keyword) corresponding to the data sheet of the component in the following format:

- Pin number (1 to 144)
- Signal name
- Model name : the generic IO model is « Ioport » ; specific Ios may have other model names (such as PWMport) ; predefined keywords are « VCC, VDD » for supply, « VSS or GND » for ground, « NC » for non connected Ios
-

Parameter	Suggested value
[Pin]	1 PP3 IOport 2 PP2 IOport 3 PP1 PWMport 4 PP0 PWMport 5 PJ2 IOport …

3.1 Physical dimensions

The package and IC physical dimensions are placed in the [Package model] section, and start by « | » to avoid parsing errors with conventional IBIS loaders. In IC-EMC the list of parameters appear in the IBIS window, by a click in "Tools → Advanced Spice & Ibis" (IBIS file should have been loaded). This tool can also be accessed from the IBIS interface. The parameters listed in Fig. 2 appear. A basic but fast 3D reconstruction of the package can be produced from the IBIS interface, by clicking on the button "3D Draw". Figure 3 presents the 3D model of the reconstructed package. The types of the package leads is indicated by different colors (red for power supply, blue for ground, yellow for general purpose I/O, grey for not connected I/O).

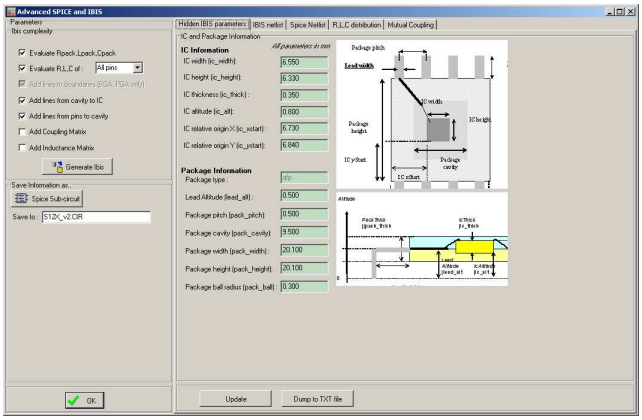


Figure 1 : Hidden parameters stored in the [package model] section of the S12X ibis file (case_study\s12x\s12x_v2.ibs)

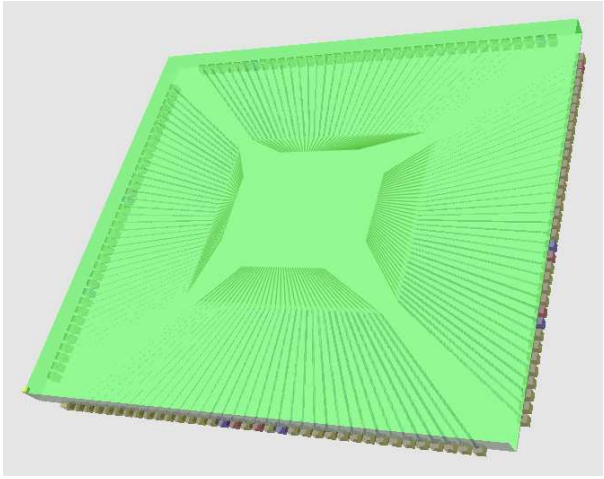


Figure 2 : 3D view of the S12X package

3.2 Package electrical parameter extraction

Precise values for R,L,C of each pin can be added to the IBIS file, as the lead length may vary significantly depending on the position in the package. The methodology for extracting more precise values for each pin is as follows:

- The IC package width, length and pitch are resourced using hidden keywords in the IBIS file, as described in Fig. 2.
- Each pin is assigned geometrical coordinates at the package border to the package center, from which the length is deduced.
- The package is modeled by a dielectric box: its effective permittivity is set according to the package material.

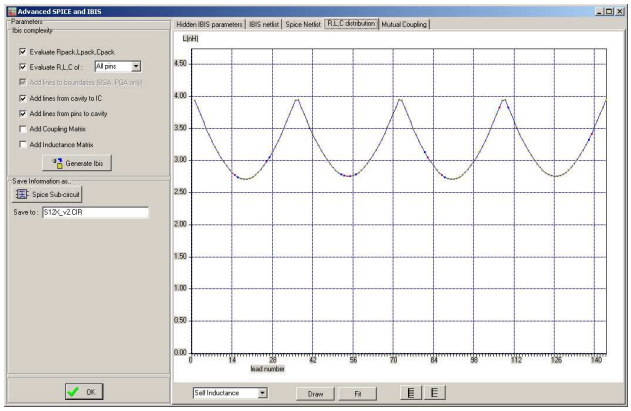


Figure 3 : The evaluation of the package inductance for each pin (Tools → Advanced Spice & Ibis)

Analytical formulations are applied to each pin to compute R, L and C (See chapter 3 and appendix G). It should be noticed that the DC resistance of the package lead differs significantly from the AC resistance. See Appendix C for more details on skin effect. The R,L,C computation is performed by IC-EMC using the command "**Tools → Advanced Spice & Ibis**". A plot of the inductance variation depending on the pin number is given in Fig. 4.

The typical, minimum and maximum values for R, L and C are computed by a click in the "Ibis Netlist". For the S12X Quad-Flap-Pack package, the result is as follows.

```
 [Package]
|           typ min max
R_pkg    0.080 0.068 0.099
L_pkg    3.191n 2.711n 3.941n
C_pkg    0.798p 0.678p 0.985p
```

You can also see the appendix H to have a more accurate evaluation of parasitic R, L and C values of package pins, based on a more precise geometrical model of package.

3.3 Test-Board Design

The test board used for EMC measurements is shown in Fig. 5. Note that the test board presents some deviations to the standards, especially with the additional small board designed for being able to measure or monitor all the pins of the microcontroller. The component is isolated on one side of the board, all other active and passive elements being on the other side of the board.

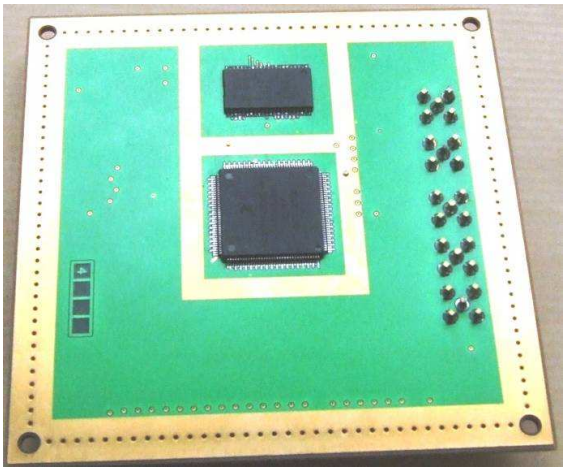


Figure 4: Top Side of the S12X test board

The configuration of the DUT for conducted and radiated emission tests is defined below:

- All ports have been configured as output with the pull-up and the reduce drive disabled.
- The output clock is not activated
- The internal PLL is activated to set a bus clock frequency at 32 MHz
- All inactive ports are set to 0x00.
- Port A is switching at a frequency of 2.27 MHz from 0x55 to 0xAA (in hexadecimal notation) with a 50% duty cycle as presented in Fig. 6.

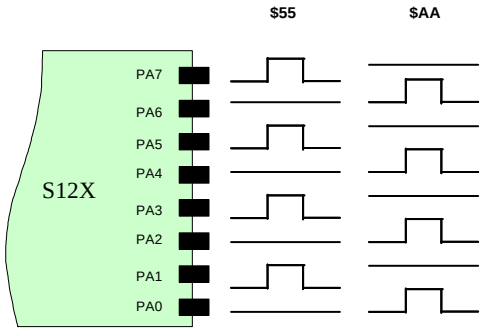


Figure 5 : The bit Port A switches from 0x55 to 0xAA at a 2.27 MHz rate

4 Microcontroller emission measurement

4.1 Radiated measurement in GTEM

The measurements have been performed using a GTEM cell. Fig. 7 presents one measurement performed for one orientation in the GTEM Cell. The maximum level of emission when the *PortA* is activated reaches 35 dBµV. The corresponding file is 's12x_tem.TAB' and corresponds to the maximum emission level of the four possible orientations in the TEM cell. In this measurement, the PLL, core and *portA* are active.

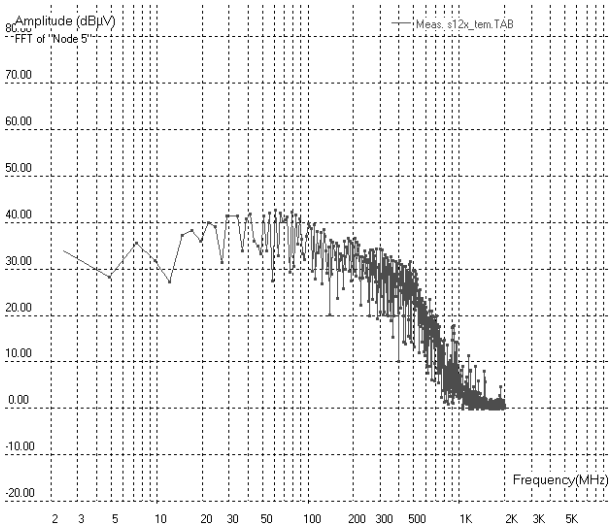


Figure 1 : GTEM Measurement for Port A and core activity (case_study\s12x\s12X_tem.TAB)

4.2 Radiated measurement in near field scan

Near-field measurements have been performed with a scan table developed at Len7 labs, France. The component is positioned on a table that can be moved automatically in the horizontal plane. The height of the probe above the IC is manually set thanks to a micrometric screw at 0.25 µm above the top of the circuit package. A set of miniature probes in coaxial technology (loops, monopoles and dipoles) have been manufactured in order to measure each component of the electromagnetic field. The magnetic field scan shown in Fig. 8 (Hx component in this case) gives interesting information about currents that flow into the IC. A calibration process has been developed so that the actual magnitude of the measured field component can be determined.

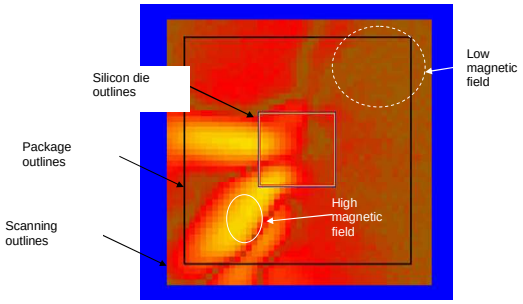


Figure 2 : Example of near-field magnetic scan of S12X (case_study\s12x\s12X_scan_Hx.len7)

5 Microcontroller Emission model

The purpose of this paragraph is to describe how a non-confidential model for the S12X microcontroller has been constructed. The global methodology is illustrated in the figure below.

5.1 Internal Activity Model

The Internal Activity model corresponds to one or more current sources (named *IA* in ICEM). The current generator represents the switching activity of the logic core. As the IC vendor did not give detailed information about the current source, the IA source was approximated by a triangular pulse (figure 9). Knowing that the operating clock frequency is 16 MHz, current peaks appear both at the rise and fall edge of the clock, which corresponds to a 31.2 ns period (32 MHz frequency). The peak current is 450 mA, which is deduced from the core complexity. A more accurate model of the current source would require a full-chip layout extraction or a high-level activity estimation based on logic cell description.

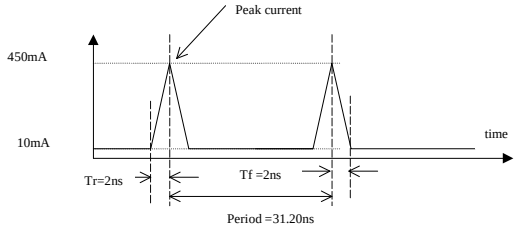


Figure 1 : The approximated current pulse used in the ICEM model for the S12X

5.2 Passive distribution network (PDN) model

The current source is associated with passive elements which model the internal power supply rails such as metal tracks and internal decoupling capacitances. The RLC elements used to build S12X passive network are listed in Table 2. Figure 10 illustrates the position of these elements and the connection with the internal activity source. The supply network model was determined from calculations using analytical formulas based on the physical dimensions of the VDD and VSS tracks.

Parameter	Description	Value
C_onchip	Distributed capacitance at the level of the sea of gates	200 pF
R_onchip	Distributed resistance between logic gates	1 ohm
Ldie_Vi	On-chip series inductance	1 nH
Rdie_Vi	On-chip series resistance	0.5 ohm

C_diedec1, C_diedec2	On-chip decoupling capacitance	0.5 nF
R_die1, R_die2	Parasitic resistance between VDD and VSS supply rails	0.5 ohm
Lpack_Vi	Series access inductance of the package	4-5 nH
Rpack_Vi	Series access resistance of the package	1 ohm

Table 1 : Description of passive network elements.

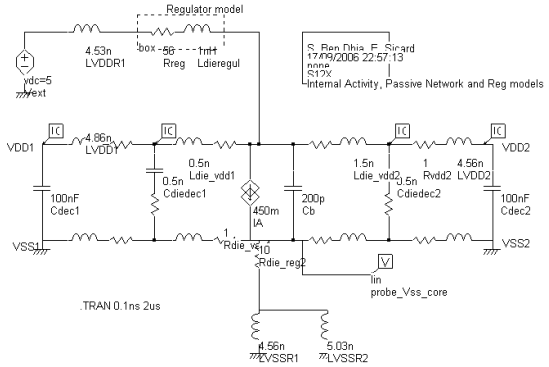


Figure 2 : The Internal Activity (IA) and Passive Distribution Network (PDN) in the S12X component (case_study\s12x\s12x_ia_pdn.sch)

The value of the on-chip decoupling capacitances *Cdiedec1* and *Cdiedec2* were provided by the Freescale design team. However, its value would have been measured externally using a Vector Network Analyser and the identification of R,L,C elements from the Z(f) curve.

5.3 Regulator Model

The value of the resistance *Rreg* – modeling the on-chip regulator – is optimized thanks to DC simulations in order to decrease the external supply 5 V voltage to 2.5 V internally. A value close to 56 Ω gives the desired result. Several authors consider that the simple resistance do not account for high frequency by-pass. A coupling capacitance *Creg_ByPass* has been added in parallel to the resistance. The serial inductance accounts for the distance (2 mm) between the regulator location and the logic core.

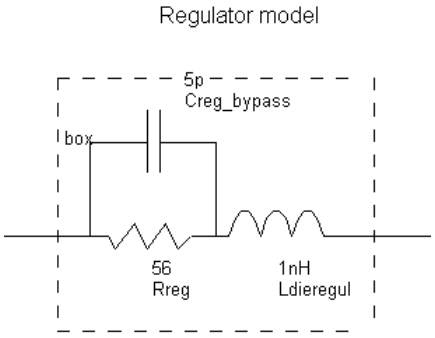


Figure 3 : on-chip regulator model

5.4 Supply Model

The digital core is fed by the internal voltage regulator through *VDDR1.* The pinout of the microcontroller is presented in Fig. 12 where *VDD*/*VSS* pins are highlighted. The VDD1 and VDD2 power supplies are connected to the internal 2.5 V core supply and are connected to external decoupling capacitances through pins *VDD1/VSS1* and *VDD2/VSS2*. Notice the 100 nF on-board CMS capacitances on schematic of internal power supply described in figure 10. For simulation purpose, initial conditions are applied to each large capacitance to avoid unnecessary transient phases for voltage stabilization. These initial conditions are controlled by “IC” probes as seen in Fig. 10. The supply pin VDDPLL is dedicated to the PLL part. The supply pin VDDA is dedicated to the ADC converters.

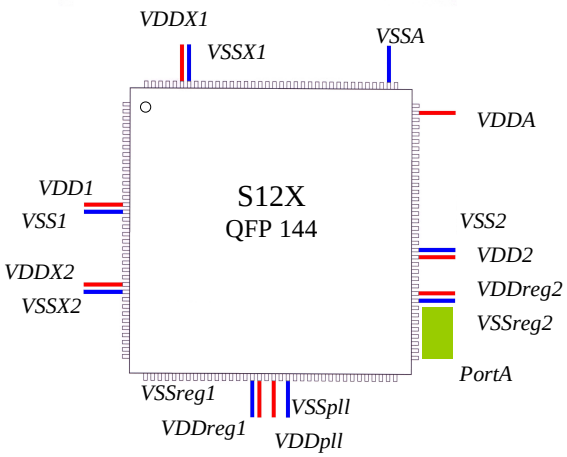


Figure 4 : The S12X supply network

Supply pins	Nominal VDD value	Description
VDD1, VSS1	2.5 V	Internal power and ground generated by the internal regulator.
VDD2, VSS2	2.5 V	Internal power and ground generated by the internal regulator.
VDDA, VSSA	5 V	Operating voltage and ground for the A/D converter. Reference for the internal voltage regulator.
VDDR1, VSSR1	5 V	External power and ground, supply to the internal voltage regulator
VDDR2, VSSR2	5 V	External power and ground, supply to the internal voltage regulator
VDDX1, VSSX1	5 V	External power and ground, supply to I/O pins.
VDDX2, VSSX2	5 V	External power and ground, supply to I/O pins.
VDDPLL, VSSPLL	2.5 V	Operating voltage and ground for the PLL. Internal power and ground generated by the internal regulator.

Table 2 : Definition of the S12X power and ground pins

The supply model must consider in priority the regulator path for the logic core (VDDreg1, VDDreg2), the ground path for the logic core (VSS1, VSS2) and the I/O supply network, although not directly connected to the core (VDDX1, VDDX2, etc). The supply model used for simulation does not consider supply pins VDDA, nor the PLL supply VDD_pll. In contrast, the ground connections VSSA and VSS_Pll are considered to take into account substrate coupling.

5.5 Input/Output model

The I/O supply network consists of *VDDX1/VSSX1* and *VDDX2/VSSX2.* Ports J, K, M, P, S, and T are supplied by through VDDX1 and VDDX2. Ports A, B, C, D, E and H are supplied by VDDR2. The active port in emission measurements is port A. A simplified model for this port is preferred to a detailed model to reduce the simulation complexity.

In other words, the 8 toggling wires are merged into a single buffer that generates an equivalent parasitic emission.

The model order reduction comprises the following steps.

- The capacitor *Cpack* corresponds to the sum of output pad capacitor.
- The inductance *Lpack* corresponds to the package and lead inductance of one single path, divided by 8.
- The capacitance *Cload* corresponds to the sum of 8 capacitance loads.

This simplified IO model described in figure 13 predicts reasonably well the rise and fall time observed with an active probe. The current consumption on the IO supply is representative of the 8 buffer switching. Furthermore, the current that flows on *Lpack* inductor is representative of the sum of 8 currents that flow in the 8 package leads.

Parameter	Description	Typical
Pull Down	NMOS which pulls down the 8 output loads in full-drive mode (reduced drive not addressed in this case study).	W= 1440µm L= 1 µm
Pull UP	PMOS which pulls up the 8 output loads in full-drive mode	W= 4320 µm L = 1 µm
Rise/Fall time	rising/falling time (measured with the active probe of a high bandwidth oscilloscope)	Td, tr=7ns

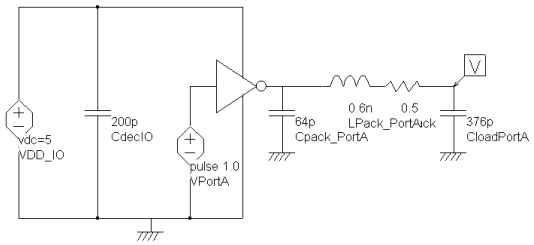


Figure 5 : Pull_Up, Pull_down modeling and resulting macro-model (s12x_portA.sch)

5.6 IC-TEM coupling model

The coupling between the IC and the TEM cell is based on two elements:

- The coupling capacitance between the septum and the core supply structure. Its value fluctuates from 10 fF to 100 fF, depending on the package size. In the case of S12X, we use Cx=20 fF.
- The inductive coupling between the package leads and the septum inductances. We use “K” coupling coefficients supported by SPICE. The maximum inductive coupling between the septum and supply leads is close to 1%.

The coupling between the VDD supply inductance *Lvdd1* and the septum inductance *Ltem1* is represented by a coupling factor K. The coupling element K is added as a label or as a specific symbol. When added as a label, the syntax is as follows. The coupling value here is 0.01, equivalent to 1%. To modify the coupling value, double click inside the label, and change the number. The coupling symbol also exists in the palette, which eases the choice of the coupled inductances and the modification of the coupling.

```
Kxxx Lyyy Lzzz coef
Example: K1 LVDD1 Ltem1 0.01
```

6 Comparison between emission measurements and simulations

6.1 Tem cell measurements vs. Simulations

Open the file called “case_study\s12x\s12x_tem.sch” (Fig. 14). The schematic contains the core of the S12X, its power supply network and an equivalent model of the 8 I/O of the port A. The microcontroller is coupled to the septum of a TEM cell.

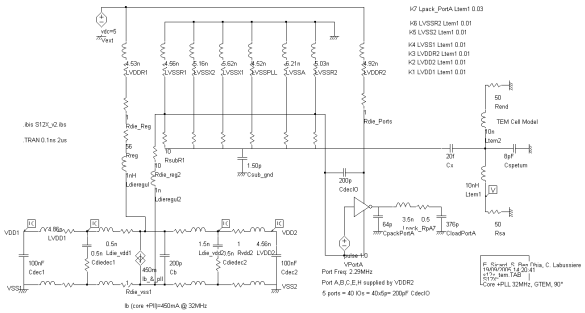


Figure 1 : Core, PDN and Port A of the S12X in a TEM cell (case_study\s12x\s12x_tem.sch)

The model is simulated in time domain. Click on “EMC → Voltage vs. Time” or on the icon  to display the voltage profile in time domain. Click on the button “Auto Fit” to fit the scale of the graph. Figure 15 presents the simulated voltage at one TEM cell terminal.

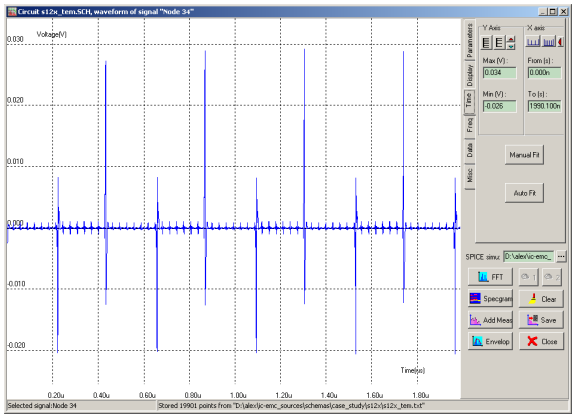


Figure 2 : Voltage induced in TEM cell (case_study\s12x\s12x_tem.sch)

The time domain profile shows that the signal is made of two contributions:

- the contribution of the I/O which switch at 2.29 MHz and creates the larger bounces
- the contribution of the core, its activity is synchronized by a 16 MHz clock

Fig. 16 gives a comparison between measurement and simulation of the S12X emission with the core, PLL and IO active. The predicted emission level is slightly higher than the measurement but fits quite correctly over the critical bandwidth 10 MHz-1 GHz. Some model parameters may be re-arranged to fit measurements more accurately. However, it should be noticed that this model is closely related to physical parameters, and that the internal current source is simply modeled as a pure triangle.

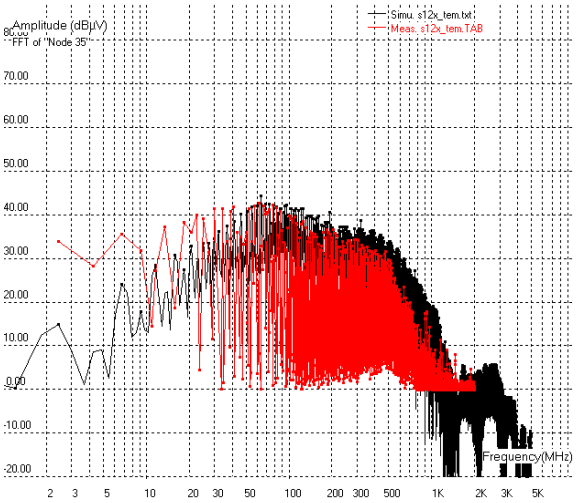


Figure 3 : TEM cell measured emission compared to simulation (case_study\s12x\s12x_tem.sch)

6.2 Near-field measurements vs. Simulations

Several scans have been performed using a variety of probes, at various frequencies. The results shown below concern the components Hx and Hy of the magnetic field, at 2.25 MHz the frequency corresponding to the *PortA* switching. Figure 17 describes the electrical model used for the prediction of the magnetic field radiated by the component. It is quite similar to the model used for TEM cell prediction, except that it includes the 8 I/Os of the port A represented individually. Besides, vertical connections of the package to the board are added to the inductances associated to the package leads.

Package leads are 0.2 mm width connector placed 0.8 mm above a infinite ground plane. Only the inductances associated to the following leads are considered:

- the 8 I/O of port A
- VDDR2 and VSSR2
- VSSR1
- VDD1/VSS1 and VDD2/VSS2

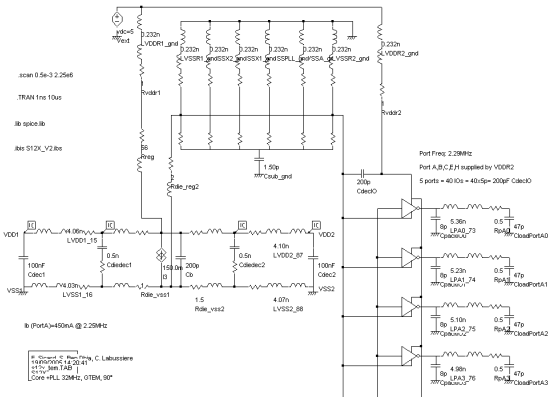


Figure 4 : Model used for near field simulation of the S12X (case_study/s12x/s12x_scan_portA.sch)

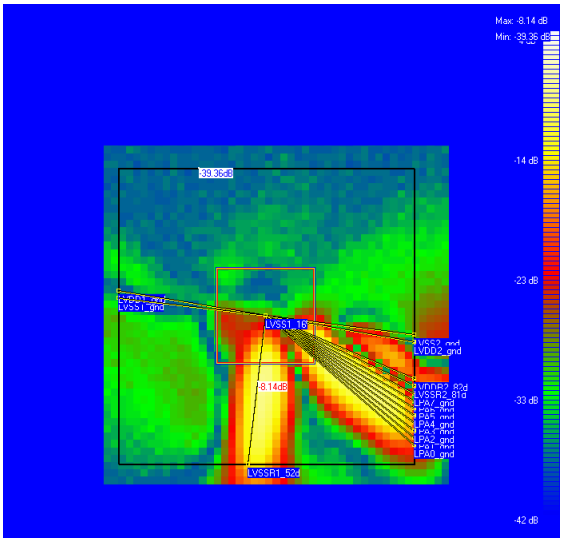
Currents that flow through these pins are related to I/O switching and core activity. The simulation is based on 15 pins or 30 radiating inductances.

Open the file "case_study/s12x/s12x_scan_portA.sch" and launch the SPICE simulation. Then open the near field simulation tool. Set the frequency to 2.25 MHz (the switching frequency of I/O) and set the scan altitude to 2.4 mm.

As the package is 1.5 mm thick, the probe is placed 0.25 mm above the top of the package and the radius of the magnetic field probe is about 1 mm, the scan altitude is assumed to be about 2.4 mm.

After selecting the current simulation file in “Simulated i(t)” field, the simulation is launched automatically. Simulation results are compared with measured scan, which are provided in the files “s12x_scan_Hx.len7” and “s12x_scan_Hy.len7”. The values of the magnetic field in the files are given in dBA/m. Move the file to superimpose the symbol of the package to the measured scan.

By clicking on the buttons “Meas. Scan” and “Simul. Scan”, you can alternatively change to one or the other scan. Figure 18 compares the measured (on the left) and the simulated Hx component of the magnetic field. The repartition of the magnetic field on the scan surface is very identical in measurement and simulation. The simulated magnetic field is a little higher than the measured field: the maximum measured Hx field is equal to -8.14 dBA/m while it is equal to -7.71 dBA/m in simulation. This discrepancy can be explained by the measurement uncertainties, the uncertainties concerning probe placement and the error of the model.



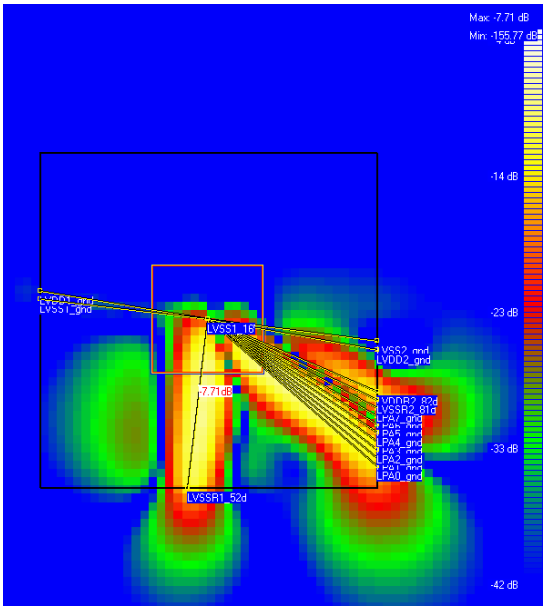


Figure 5 : Comparison between measured and simulated Hx field radiated by the S12X (s12x_scan_Hx.len7)

Figure 19 compares the measured (on the left) and the simulated Hy component of the magnetic field. Once again, a good matching is observed between measurement and simulation both for the near-field map and the amplitude of magnetic field. The maximum measured Hy field is equal to -8.83 dBA/m while the maximum simulated Hy field is equal to -6.84 dBA/m. More comparisons between measurements and simulation on the S12X device may be found in [5].

As magnetic field emission is related to circulation of current, these simulations are very interesting because they show through which pins the current associated to circuit activity flows and give a direct information about ground return path of the current. Port A I/Os are supplied through VDDR2 and VSSR2 pins, which is confirmed by the near field scan measurement. The two hot spot observed in measurement are located above Port A I/Os and VDDR2 and VSSR2 pins.

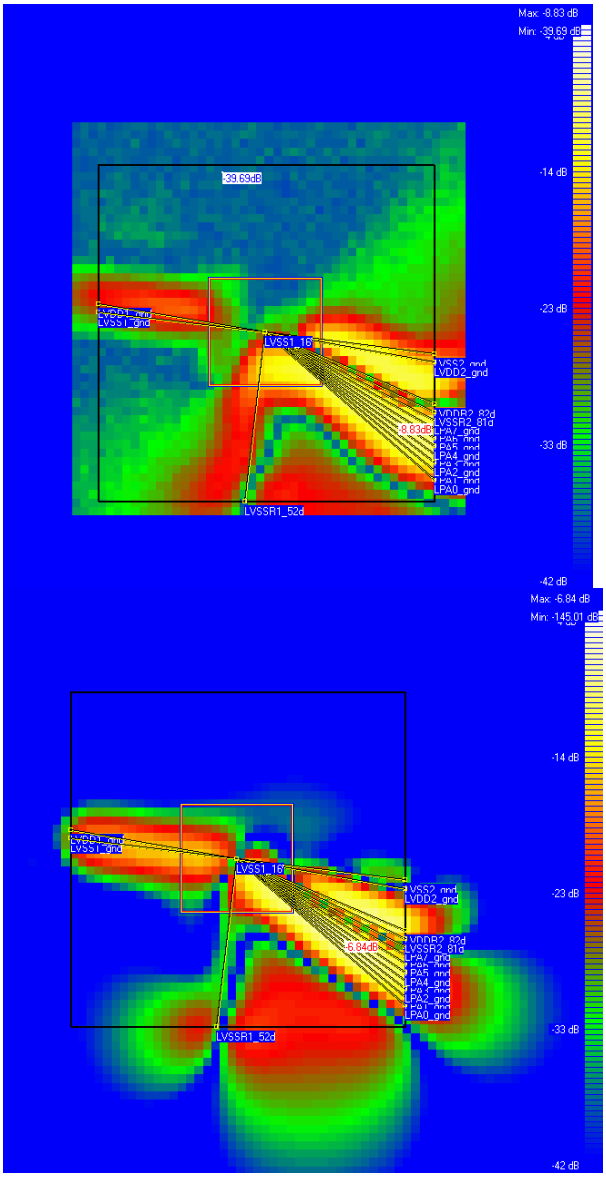


Figure 6 : Comparison between measured and simulated Hy field radiated by the S12X (s12x_scan_Hy.len7)

However, two other hot spots with smaller peak amplitude are observed above VSSR1 and VSS1 pins. Some current might flow through VSS2 pins but this pin is placed too close to the VDDR2/VSSR2 pins so that the spot induced by current flowing through VSS2 pin is hidden by the spot due to VDDR2 and VSSR2 pins. This measurement proves that a small part of the current used to supply the I/Os does not return to the ground through VSSR2 pins but flows through VSSR1, VSS1 and certainly VSS2.

Some parasitic paths certainly due to substrate coupling can explain the existence of these parasitic ground return paths. They can have major consequences on EMC of the circuit since the activity of a block can parasite an other block. Moreover, in order to reduce efficiently both the conducted and radiated emission, ground return path for the current must be exactly known. It allows a judicious placement of decoupling capacitors and an adequate routing strategy to reduce RF current loops.

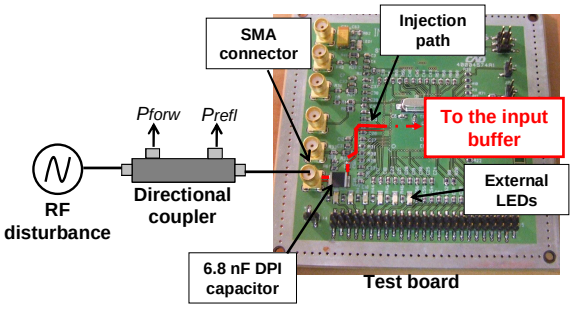
7 Simulation of DPI on an I/O port

In this section, we present a comparison between measured and simulated susceptibility of an I/O port of the S12X microcontroller to direct power injection.

7.1 Set-up of the aggression of the I/O port

One I/O of the microcontroller configured as an input is disturbed and its conducted susceptibility is characterized. Figure 20 describes the test set-up. The microcontroller is mounted on the same test board as the one used for emission characterization. A 6.8 nF coupling capacitor is placed as close as possible to the I/O under test. A RF harmonic aggression is produced by a signal synthesizer connected to a 10-W power amplifier. The RF disturbance is applied to theI/O input through a DPI capacitor and a directional coupler and a 50-Ω adapted SMA connector.

A test software has been placed in the program memory of the microcontroller which reads the pin state regularly and copies the logic information to another I/O configured as output. A LED connected to the output port displays the logical state of the sampled information. The normal state is 0, which stuck the LED to an off state.



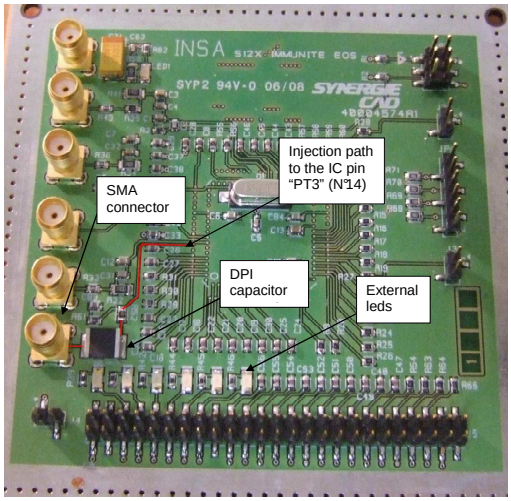


Figure 1: DPI test setup applied to the microcontroller I/O port

When the applied disturbance is sufficient to modify the logical state into an erroneous 1, the LED will light on, which corresponds to our susceptibility criterion.

7.2 Measurement results

Figure 21 presents the measurement results corresponding to the I/O port susceptibility, represented in terms of forward power versus frequency (*case_study\s12X\S12X_dpi.tab)*. The maximum injected power is limited to 25 dBm. The susceptibility threshold tends to increase with frequency, especially above 800 MHz.

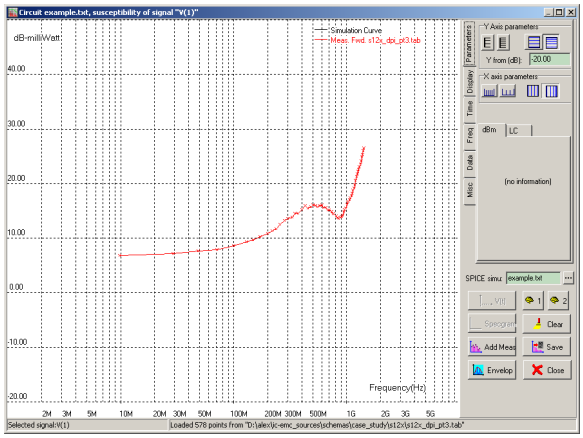


Figure 2: DPI on I/O result

7.3 I/O susceptibility modeling

Several parts are essential for the accurate modeling of the IO susceptibility. The schematic in figure 22 presents the different blocks which have a major influence on the susceptibility. The first block is the signal generator and the coupler. The coupler model enables the simulation of the forward power. The coupling path model is also critical as it immediately follows the coupler and affects the propagation of the conducted RF disturbance.

The RF disturbance flows from the RF source to the amplifier, through the coupler, the DPI capacitor, the printed-circuit-board tracks, the package lead, bonding and eventually to the buffer. The on-chip buffer is connected to its own supply network which propagates the injected noise within all the circuit.

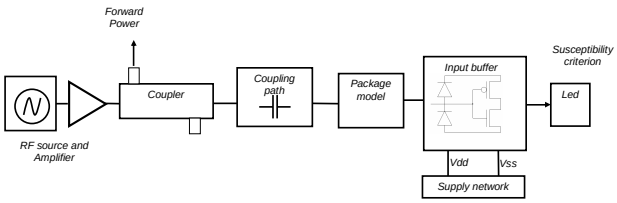


Figure 3: General schematic of IO susceptibility modeling

7.4 Coupling path model

A measurement of the DPI coupling path has been performed using a vector network analyzer. The S12X pin is PT3 (pin 14). The Z(f) measurement is given in Fig. 23. It corresponds to the impedance of the complete injection path starting from the SMA connector that can be seen at the left-lower corner of Fig. 20. The model detailed in figure 23 includes the SMA connector, the DPI capacitor, the PCB tracks, the package model and the input buffer impedance.

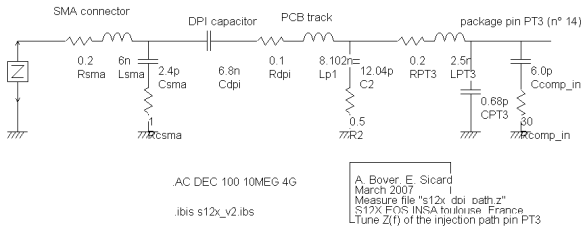


Figure 4: DPI injection path impedance (case_study\s12X\s12x_dpi_path.sch)

The SMA connector model comprises a combination of R,L and C elements. The DPI model is simply a 6.8nF discrete device. The PCB track values are computed using Delorme formulations (35 µm copper wire, 350 µm width, 25 mm length). The package pin model is derived from the IBIS information. The on-chip input capacitance called Ccomp_in is set to 6 pF according to the data-sheet and the IBIS model. The model of the IC supply network is not included for simplification reason.

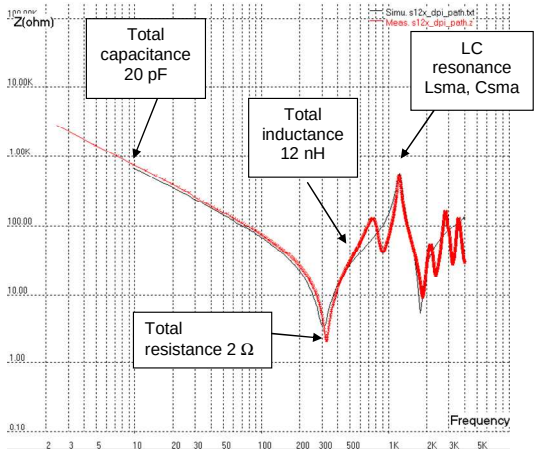


Figure 75: Comparison between measured (s12X_dpi_path.z) and simulated input impedance (s12x_dpi_path.sch)

Figure 24 shows the comparison between measured and simulated input impedance. The simulation result exhibits a very good agreement with the measurement up to 4.0 GHz. Minor resonances and anti-resonances do not appear in the simulation. The capacitance effect corresponds to the sum of all capacitances to ground (Csma, C2, CPT3, Ccomp_in), while the inductance effect starting 300 MHz corresponds to the sum of all serial inductances of the DPI path on the PCB (Lsma, Lp1, LP3).

7.5 IO model

The S12X input structure has been presented in Section 4 of this manual. The input protections include two clamp diodes for which an accurate DC model has been obtained, valid from –VDD to 2.VDD. The schematic diagram used for DC tuning of the clamp diodes is recalled in Fig. 25.

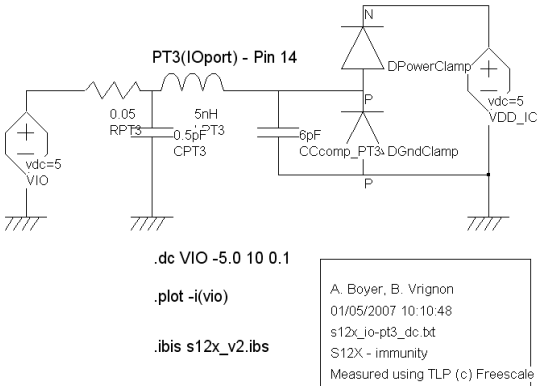


Figure 6 : DC simulation setup to tune protection diode clamping effect (case_study\s12X\S12X_io_pt3_dc.sch)

7.6 Simulation of the IO susceptibility using the IO model only

A RFI source and a directional coupler are added at the input of the coupling path. The output impedance of the RFI source is set to 50 Ω and the delay coupler is 2 ns, corresponding to a 40-cm delay line embedded in a dielectric of permittivity 2.2. The failure criterion is declared by the label ".fail 2.5" (2.5V at the voltage probe situated at the right of the schematic diagram). Figure 26 describes the schematic of the proposed model. This is a simple and entirely passive model

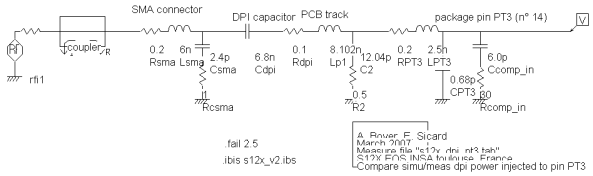


Figure 7: Model for simulating the S12X input buffer susceptibility to DPI (case_study\s12X\s12X_DPI_pt3.sch)

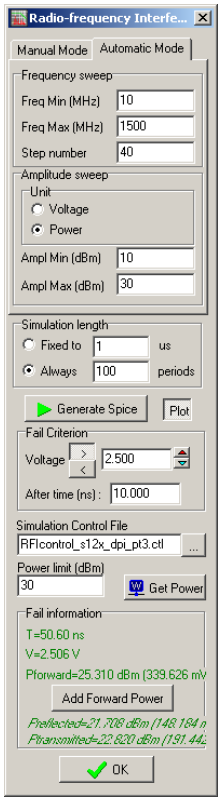


Figure 8: Configuration of the RFI interface

As described in section 7 for the DPI simulation on a 330 Ω resistor, the susceptibility simulation is automatically controlled by the RFI interface menu. The RFI window opens by clicking "EMC → Susceptibility dBm vs. frequency" or the icon "Susceptibility dBm vs. frequency ".

Select the desired frequency and amplitude sweeping for the RFI. The frequency is swept between 10 MHz and 1.5 GHz. The amplitude is swept between 10 and 30 dBm. Set the SPICE duration equal to 100 periods. This option sets a transient simulation period which depends on the RFI frequency. If the duration simulation is constant, it can be too short for low frequency and inversely too large for high frequency. This option is adapted for simulation over wide frequency range. Figure 27 describes the configuration of the RFI interface to control the susceptibility simulation. Then click "Generate Spice", open WinSpice, load and simulate the file "S12X_DPI_pt3.CIR".

Once the simulation is complete, click “Get Power” and “Add Forward Power” to display the susceptibility threshold. Click on the button “Add Meas” to display the measured susceptibility threshold and choose the file “*s12X_dpi_pt3.tab*”. Figure 28 presents the comparison between the measurement and the simulation.

The measured forward necessary to induce a logic fault in the S12X pin PT3 is significantly less than the once predicted in the simulation, as seen in Fig. 28. This is mainly due to the fact that no real IC model has been provided in the schematic diagram, except the buffer input capacitance Ccomp_in.

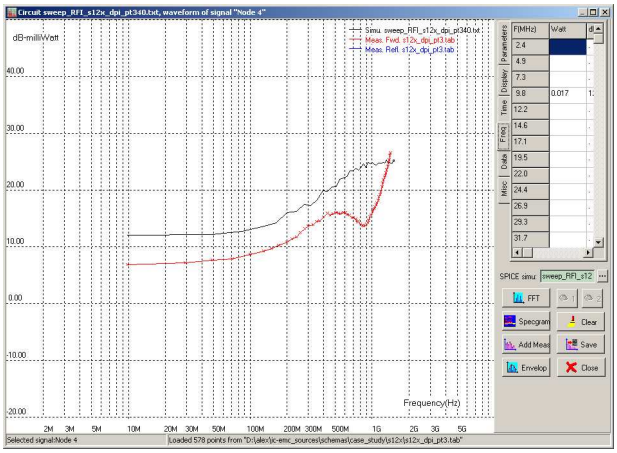


Figure 9 : Comparison between measured and simulated susceptibility (S12X_dpi_pt3.sch, s12X_dpi_pt3.tab)

7.7 Simulation of the IO susceptibility using the PDN

In this paragraph, we connect the Passive Distribution Network corresponding to the IO supply to the S12X input pin, as shown in Fig. 29. We run again an automatic simulation of the immunity, keeping the same parameters for the RFI source and the same voltage failure criterion of 2.5 V at the input pin. As can be seen in the comparison between simulation and measurements (Fig. 30), the passive supply network influences the IC susceptibility in such a way that the susceptibility curve gets closer to the measured result.

A more complex model including the full passive distribution network of the core has been developed by A. Boyer [4] with very close correlation between measured and simulated IO immunity (Fig. 31).

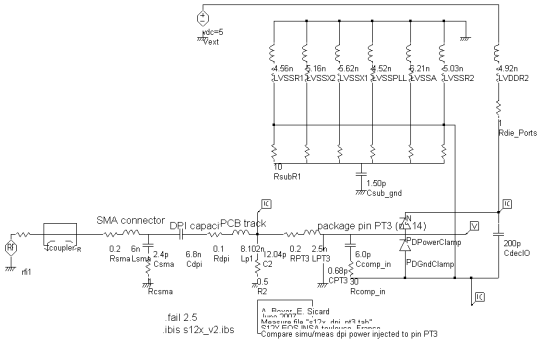


Figure 10 : S12X input immunity simulation using the IO PDN (case_study\s12X\s12x_dpi_pt3_iosupply.sch)

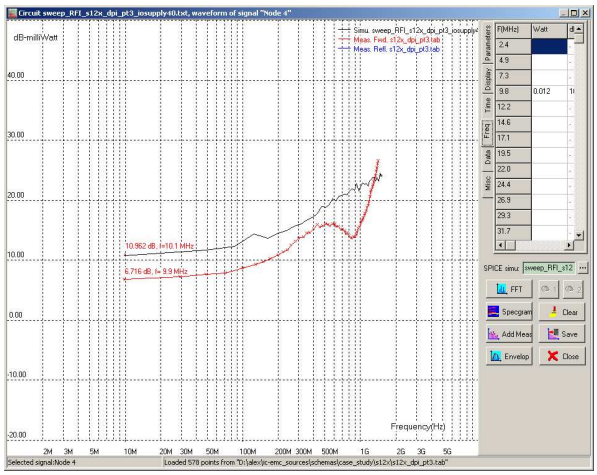


Figure 11: Simulation of the IO susceptibility from 100 MHz to 2 GHz (case_study\s12X\s12x_dpi_pt3_iosupply.sch)

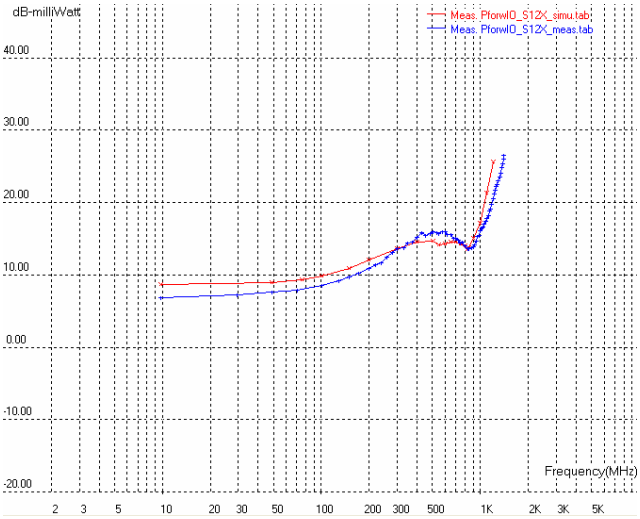


Figure 12: Comparison between measured and simulated S12X IO susceptibility using a full IC model [4]

8 Summary

In this S12X microcontroller case study, we achieved a correct matching between emission measurements and simulations, which demonstrates the ability of a simple ICEM-based model to handle the conducted and radiated emission prediction of complex microcontrollers. Moreover, the same kind of model was used to predict the susceptibility of one block of the microcontroller. A simple model allows a rapid evaluation of the susceptibility level of a circuit. More in-depth studies of this component may be found in [2] to [5].

9 References

[1] Freescale S12XD: 16-bit Automotive Microcontroller. More information available at http://www.freescale.com

[2] Ben Dhia S., Joly J., Lochot C., Labussière, C., 2005, A 16 bit Microcontroller emission measurements and modeling using different approaches and a specific test board, EMC Compo 05, Munich, Germany.

[3] C. Labussière, S. Ben Dhia, E. Sicard, J. Tao, H. J. Quaresma, C. Lochot, B. Vrignon, "Modeling the Electromagnetic Emission of a Microcontroller Using a Single Model" IEEE Transactions on EMC, 2008, pp 22-34, vol 50, n°1.

[4] A. Boyer, S. Ben Dhia, E. Sicard "Modelling of a Direct Power Injection Aggression on a 16 bit Microcontroller Input Buffer", EMC Compo 07 Torino, Nov 2007, Italy, pp. 35 – 39

[5] C. Labussiere, , E. Sicard, S. Ben Dhia "PREDICTING THE NEAR-FIELD RADIATION FROM AN INTEGRATED CIRCUIT", EMC Europe 2006, International Symposium on Electromagnetic Compatibility, Barcelona, Spain, September 2006