



# Near-field emission prediction of CESAME

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**Abstract:** The purpose of this case-study is to compare the measured near-magnetic field with the simulated field. The CESAME test pin out chip has been described in an IBIS format, which includes details on the package parasitic R,L,C. In parallel, the electrical model of the core and supply network is given by the ICEM model. The concept of radiating inductance is detailed, with the step-by-step procedure to simulate the magnetic near-field using IC-EMC.

*This work has been conducted in cooperation with ST Microelectronics (Crolles, France) and EADS, within the frame of the European project MEDEA+ “MESDIE”.*

*Keywords: near-field scan, emission prediction, localization of ground return current, ICEM model, substrate coupling*

## 1 Introduction

The CESAME test chip has been designed by ST-Microelectronics in cooperation with INSA Toulouse for the characterization of conducted and radiated emissions from six identical logic cores, each having a specific design technique which aims to reduce parasitic emissions. The main goal of the test chip was to validate these design rules and to quantify the benefits in terms of reduction of parasitic interferences. The most interesting results have been presented in [1][2][3].

The internal structure of CESAME is outlined in Fig. 1. Six logic core blocks are implemented in the same die. All these blocks have an identical structure based on latches, a clock tree and standard gate which reflect a standard core activity.

Among these cores, two structures are worth of interest in our study: the normal core called “NORM” which is supposed to be noisy, and the “RC” core with includes a series resistor on the supply tracks and a local on-chip decoupling to feature low parasitic emission.

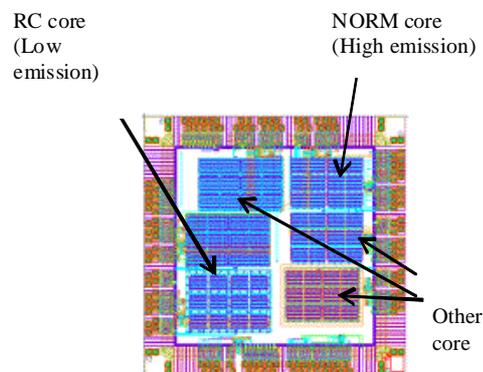


Figure 1: The CESAME test chip



An electrical model has been setup for conducted and radiated emission prediction.

The purpose of this study is to compare the measured near-magnetic field with the simulated field. The CESAME test pin out chip has been described in an IBIS format, which includes details on the package parasitic R,L,C. In parallel, the electrical model of the core and supply network is given by the ICEM model.

## 2 Approach for radiated emission simulation

### 2.1 Proposed flow

The proposed flow is illustrated in Fig. 2. The near-field scan of the component is compared to the simulated scan, based on the radiation of package inductances. The excitation of these inductances is the current extracted by time-domain SPICE simulations. IC-EMC is used for positioning package inductances in 3D, and to calculate the H, E field from SPICE simulations.

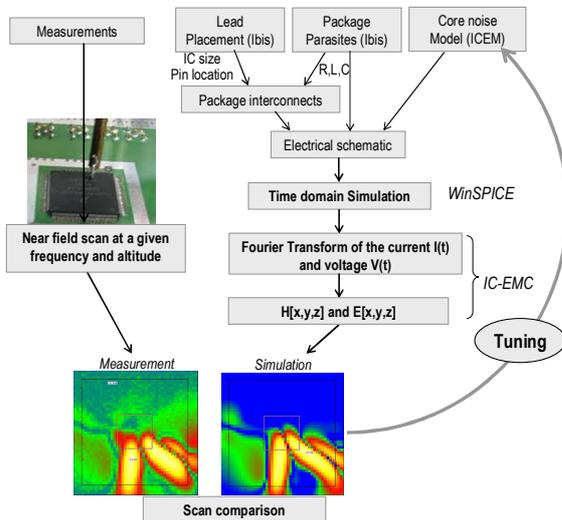


Figure 2: Flow for comparing predicted and simulated magnetic field scans

### 2.2 Reuse of the conducted emission model

The model developed to predict conducted mode using 1/150Ω method and radiated emission in TEM cell is reused. The model is presented in figure 1 [1].

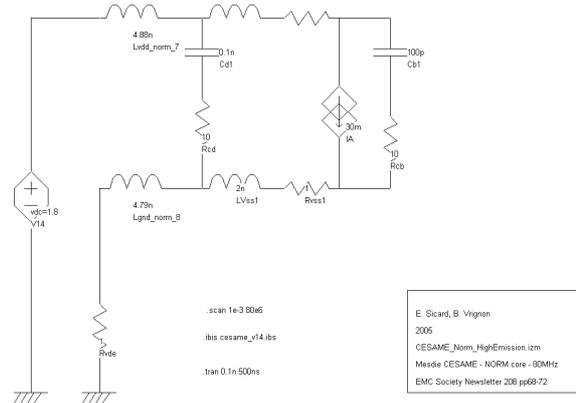


Figure 1 : The schematic diagram of CESAME used for near-field scan prediction (case\_study/CESAME/cesame\_norm\_scan.sc h)

### 2.3 Declaring inductance coordinates in 3D

The first step consists in associating geometrical model of the package to the electrical schematic through the “radiating inductances”. Table 1 describes the different steps to update the schematic and declare geometrical model of the package leads. Coordinates of inductance can be defined by double clicking on inductance symbol and checking “Assign coordinates for near-field scanning prediction” (Fig. 2). Simple geometrical models composed of a line in XY plane are used to describe package leads.

The key idea of the magnetic field simulation is to consider the CESAME circuit as a set of current dipoles. Each dipole is associated to one particular package lead inductance. This means that in first approximation, each core of the CESAME test chip may be represented by two dipoles, one for the VDD current, one for the VSS current. The current flowing inside the IC itself is neglected. Only remains the lead current.



Step	Action	Method	Comments
1	Load Ibis file	Text ".ibis cesame_v14.ibis" added in the layout	Enables the automatic loading of the list of pins, IO models and hidden keywords.
2	Reconstruct package	Click "EMC → Ibis Interface". Select the item "Package".	The pin list and hidden keywords are used to reconstruct the physical dimensions of each lead.
3	Select inductances	Assert the option "Assign [X,Y] Coordinates".	For each selected inductance (here LVdd and LVss),
4	Assign coordinates	Select the corresponding pin in the IBIS pin List	Select LVdd_norm (pin 7), and LVss_norm (pin 8)
5	Update L value and [X,Y]	Click "Update L and [X,Y]". For GND pins, click "Exchange" so that the start point is the die, the end point the package.	Apply to LVdd_norm (pin 7), and Lgnd_norm (pin 8). Click "Exchange" for "Lgnd_norm".
6	Update orientation, altitude and width	Choose horizontal or vertical orientation of the dipole. For an horizontal dipole, altitude in the XY plane is constant above the ground plane, while for a vertical dipole, the start and stop altitudes are given. The start and stop depends on the current orientation through the dipole. If the width is not given, a default width of 1 mm is used.	For both inductance, select "On the plane XY". Set the altitude to 1 mm and the width to 0.2 mm

Table 1: Procedure to assign geometrical coordinates to "radiating inductances"

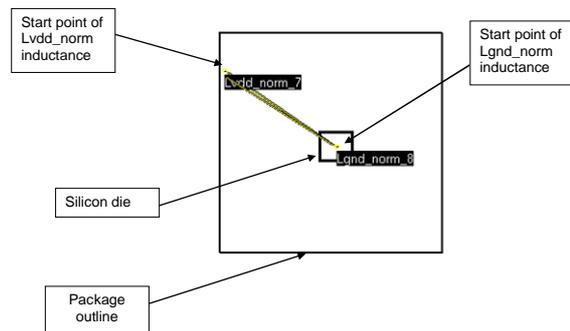
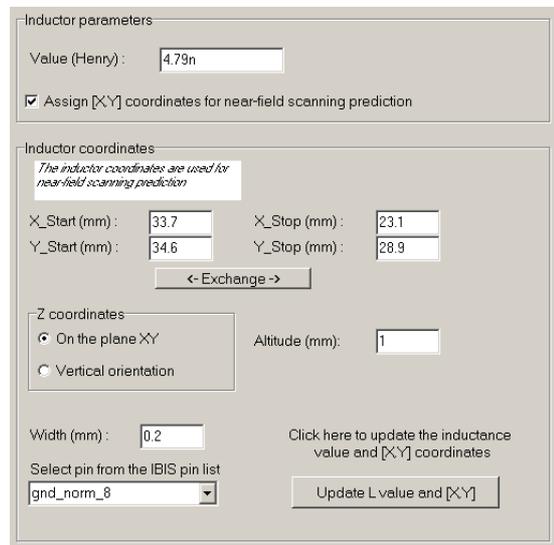
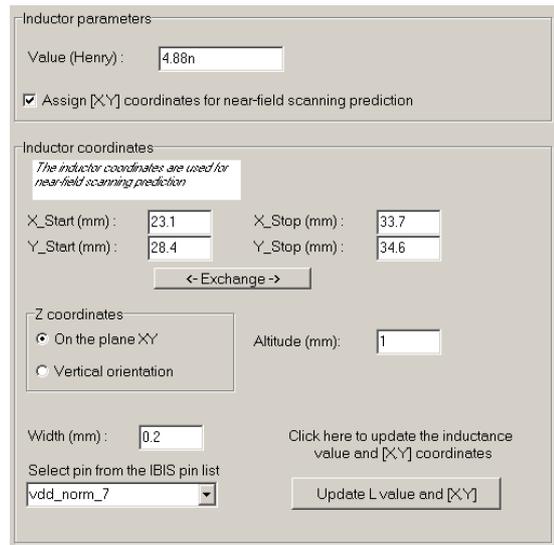
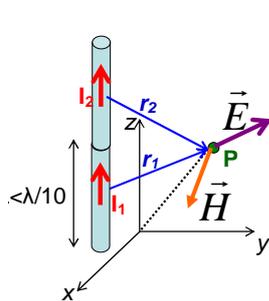


Figure 2: Define inductance coordinates and sign (case\_study/CESAME/cesame\_norm\_scan.sc h)



Step	Action	Method	Comments
6	Generate Spice File	Click "EMC → Generate Spice file" or the "Generate Spice File" icon	Creates the Spice-compatible file "cesame_norm_scan.CIR". The declared output waveforms are I(LVdd_norm_7) and I(LGnd_Norm_8).
7	Execute the Spice File	Launch WinSpice. Click "File → Open" and load cesame_norm_scan.CIR.	The currents I(LVdd_norm_7) and I(LGnd_Norm_8) and the voltage across these inductances are computed.
8	Load the SPICE Compute the radiated field	In the SPICE window, click the icon "Near Field Scan". Ensure that the result file "cesame_norm_scan.TXT" is selected in "Simulate H field" "use file". Unselect the box "Simulate E field".	The currents I(LVdd_norm_7) and I(LGnd_Norm_8) are loaded. The FFT of the currents is computed. Only magnetic field are computed, E field are ignored in this example.
9	Tune scan parameters	In the scan window, select Hx, Hy or Htotal. Change the scan altitude. Click "Simul. Scan" to compute the field.	By default the total magnetic field is computed. The scan altitude is 2mm, the frequency is defined by the keyword "scan <step> <freq>". The scan frequency is 80 MHz.

Table 2: Procedure to simulate electric and magnetic field from SPICE simulation



$$\vec{A} = \frac{\mu}{4\pi} \times \int_{-L/2}^{L/2} I(z) \frac{e^{-j\beta r}}{r} dz \vec{z}$$

$$\Phi = \frac{1}{4\pi\epsilon_0\epsilon_r} \times \int_{-L/2}^{L/2} Q(z) \frac{e^{-j\beta r}}{r} dz$$

$$\vec{H} = \frac{1}{\mu} \nabla \times \vec{A}$$

$$\vec{E} = -j\omega\vec{A} - \nabla\Phi$$

Figure 4: Electric and magnetic field formulations with the thin wire approximation

Once the geometrical model has been define, simulation of electric and magnetic fields can be launched. Table 2 describes the procedure, which starts with a SPICE simulation and an extraction of current along "radiating inductances", followed by a computation of electric and magnetic fields with IC-EMC (Fig. 3). Click on "EMC

→ Near field scan" or on icon  to start the near field scan simulation tool. In this example, only the magnetic fields are considered. The magnetic field generated by of each elementary current dipole is calculated from the formulation reported in figure 4. The formulations of the magnetic field are only valid if the dipole length is much shorter than the distance r to the observation point. As the scan was performed at the altitude of 2mm, the current dipole length is set to 500µm.

## 2.4 Simulation Results

The WinSPICE simulation is performed in time domain in order to monitor all currents flowing in all inductances. For each current  $I(t)$ , a Fast Fourier Transform is automatically performed to extract the current amplitude  $I_0$  to be injected in the dipole equation, at a given pulse  $\omega$ . In the case of the NORM core, the IC-EMC user interface shown in figure 5 displays the position of the die, the package, and the position of the two main current dipoles. The SPICE simulation result is reported in the upper right corner of the window. At 80 MHz, the current amplitude is close to 5 mA along VDD and VSS pins. The maximum total magnetic field is about -11 dBA/m, located near the leads. Change the H field component by selecting "Hy (dBA/m)" in the field "Compute" (Fig. 6). The maximum amplitude of the Hy field is equal to -15.74 dB A/m.

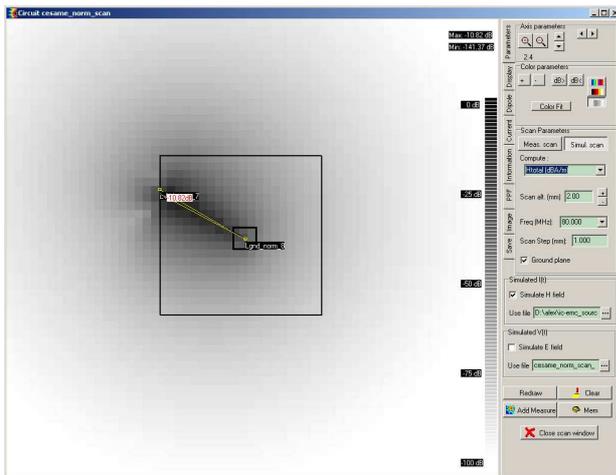


Figure 5: The simulated magnetic field  $H_{total}$  for CESAME NORM core (case\_study/CESAME/cesame\_norm\_scan.sc h)

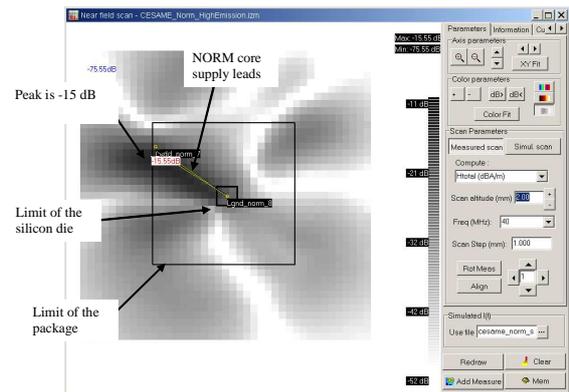


Figure 7: Measured magnetic field  $H_x$  for CESAME NORM core (CESAME\_Norm\_HighEmission.izm)

Three other regions exhibit magnetic field around 20 dB lower than the main region.

Differences between measurement and simulation come from two reasons:

- The current produced by the core NORM flows also through other pins than VddNorm and VssNorm
- The model of the leads can be improved

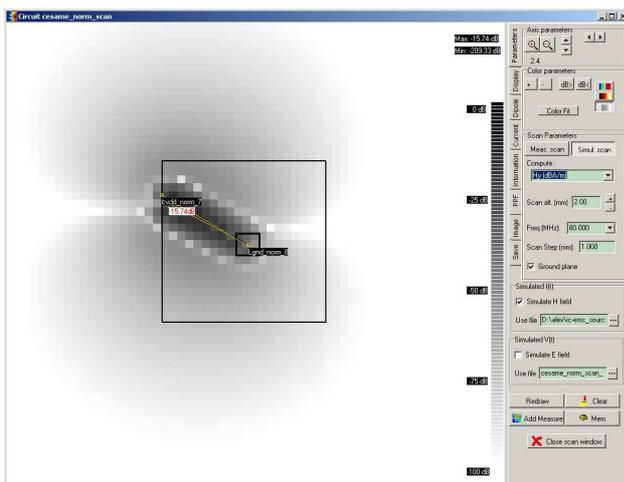


Figure 6: The simulated magnetic field  $H_y$  for CESAME NORM core (case\_study/CESAME/cesame\_norm\_scan.sc h)

## 2.5 Measurement Results

The measurement of the magnetic field has been performed on the CESAME test chip by A. Tankielun. Use “Rotate Meas.,” “align” and the arrows to align the measurements to the package as shown below. The  $H_x$  contribution of the magnetic field measured at 2 mm above the ground plane is shown in figure 7. The peak magnetic field is  $-17$  dB near the main dipole.

## 3 Multiple Return path model

It has been observed [2] that the return path of the ground current is not only the VSS pin of the core but also the other VSS connections of other cores, due to a common substrate. The coupling via the substrate is considered in the model shown in figure 8 as a resistance, which has been characterized in DC to a value of  $30 \Omega$ .

The three inductance paths correspond to the GND connection of three other cores implemented on the same die, and thus sharing the same silicon bulk. Three package inductances are added to the schematic diagram and declared as radiating elements.

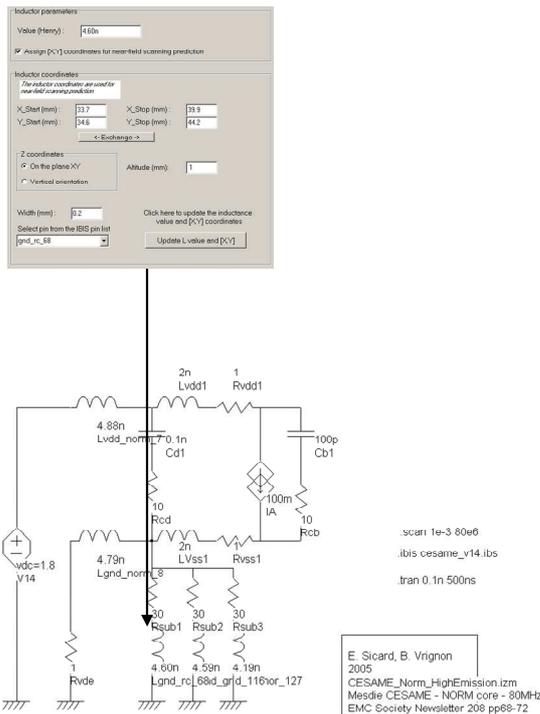


Figure 8 : The multiple return paths for the current due to the shared substrate (case\_study/Cesame/cesame\_norm\_scan\_multiVss.sch)

The simulation starts to behave closer to the measurements, as shown in figure 9. The simulation is based on one VDD current dipole and four VSS current dipoles. The magnetic field appears above each lead, which is somehow what we measure on the surface of the IC.

### References

- [1] B. Vrignon, S. Bendhia, L. Courau, E. Sicard, "CESAME: a Test Chip for the Validation of a parasitic Emission Prediction Flow in 0.18  $\mu\text{m}$  CMOS Technology", 2004 International Symposium on Electromagnetic Compatibility, 9-13 August 2004, pp 372-376, vol. 2
- [2] E. Sicard, A. Boyer, A. Tankielun "On the Prediction of Near-field Microcontroller Emission", proceedings of the IEEE International Symposium on EMC, Chicago, Aug 2005
- [3] Adam Tankielun, Peter Kralicek, Uwe Keller, Etienne Sicard, Bertrand Vrignon "Electromagnetic Near-Field Scanning for Microelectronic Test Chip Investigation", IEEE EMC Society Newsletter, Oct. 2006.

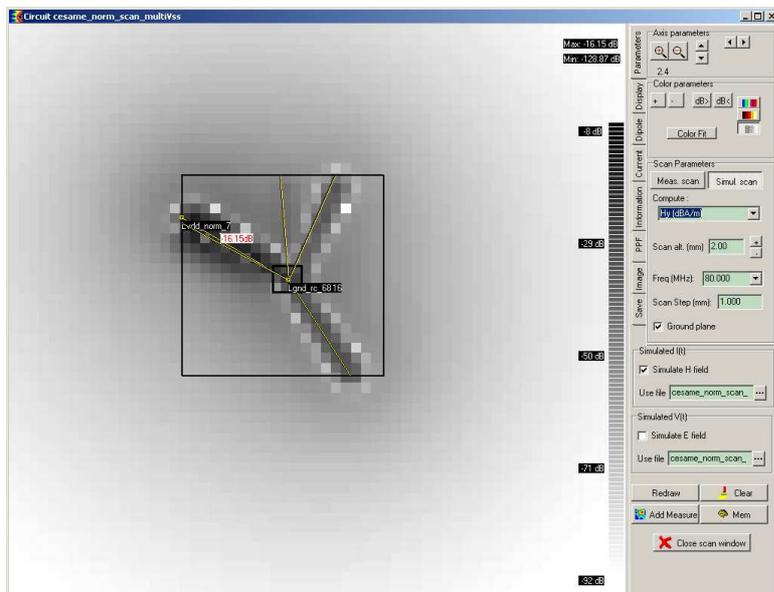


Figure 9: The simulated (left) and measured (right) magnetic emission of the NORM core in CESAME test chip (case\_study/Cesame/cesame\_norm\_scan\_multiVss.sch)