Modelling of conducted noise propagation through the power distribution network of a phase-locked loop

A. Boyer

LAAS-CNRS, INSA-GEI, 135 Av de Rangueil

31077 Toulouse – France

Contact : alexandre.boyer@insa-toulouse.fr – web site : www.ic-emc.org

Abstract: This application note presents the modelling process of the power distribution network of a phase-locked loop. This is a fundamental part of the susceptibility model of an integrated circuit to predict the amount of conducted interference coupled within the chip

This work has been conducted by A. Boyer, in cooperation with B. Vrignon from Freescale Semiconductor.

Keywords: IC immunity modeling, Direct Power Injection, Power Distribution Network modeling

Files of this case study can be found in "case_study\pll_pdn".

1 Introduction

Susceptibility of integrated circuits (ICs) is strongly correlated with:

- The intrinsic sensitivity of a circuit to voltage fluctuations across its terminals
- The propagation of (external or internal) interferences up to circuit terminals

The proposed case study is focused on the propagation of external conducted interferences into a phase-locked loop (PLL). The power distribution network (PDN) is a privileged coupling path for conducted interferences. In typical electronic applications, the PDN structure is complex, as it includes on-board voltage regulator, PCB power planes, tracks and via, on-board decoupling capacitors, package interconnects (lead, ball, bonding…), I/O pads, IC interconnects, on-chip decoupling capacitors… Thus the PDN has a frequency dependent behavior due to all these elements. Depending on the impedance of the PDN, interference coupling can be more or less efficient, which affects directly the susceptibility of the circuit to disturbance coupled on its PDN.

This case study has several objectives: first, presenting the construction of a passive equivalent model of the PDN of the PLL up to 1 GHz from S parameter measurements. The case study is only focused on the circuit PDN. Details about this model can be found in the article [1]. Then, this model should be sufficient to predict the amount of conducted interference coupling within the circuit (in case of small signal amplitude). In order to prove it, internal voltage measurements have been performed [Boyer11] to characterize the amount of external conducted interferences coupling on PLL power supply. A comparison between measurements and simulation based on the extracted PDN model will be presented to confirm the relevance of the model to

predict accurately the amount of external interferences coupled within the circuit. We will introduce the notion of conducted interference coupling which depends on the impedance of board and circuit impedance. The analysis of circuit and board impedance will help us to understand the origin of efficient coupling of external conducted disturbances observed at particular frequencies.

2 Phase-locked loop presentation

The proposed study is focused on a PLL designed in the 0.25 µm SMARTMOS from Freescale Semiconductor (Toulouse - France). Fig. 1 presents the PLL schematic. The PLL is based on a first order filter, and made of three sub-blocks (phase detector, voltage-controlled oscillator (VCO) and frequency divider) which have separated power supply pairs. The VCO is a delay-controlled ring oscillator, designed to operate nominally at 112 MHz, the frequency divider divides by 4 the VCO frequency. During experimental tests, the reference signal applied on PLL input has a frequency of 24 MHz.

This circuit is very sensitive to electromagnetic interferences, especially to voltage fluctuations induced on its PDN. For example, let's suppose that the power supply of the VCO is disturbed. The power supply voltage fluctuations are able to modify the characteristics of the VCO. The VCO can be considered as a frequency modulator commanded by its power supply fluctuations. In other words, VCO is extremely sensitive to power supply fluctuations because they increase the phase noise level or jitter amount at the VCO output. The PLL phase noise depends on the closed loop frequency response of the PLL (linked to the frequency response of the different subblocks of the PLL) [1]. Actually, VCO usually shares the power supply with the other PLL subblocks so that phase noise is also generated at frequency divider and phase detector outputs. PLL are also extremely sensitive to noise coupled on ground and substrate nodes.

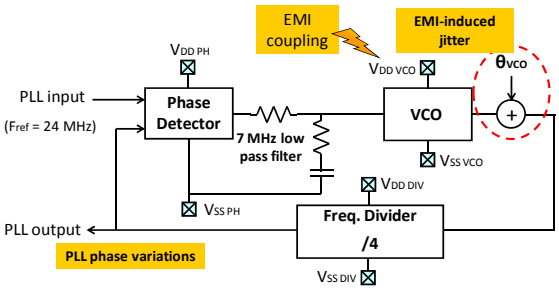


Figure 1: Phase-locked loop description

Consequently, the modeling of PLL power distribution network is critical in susceptibility prediction. The PLL power distribution network of this case study is unconventional since VCO, phase detector and frequency divider are separated. But the separation of these power supplies has been chosen to characterize and model internal coupling between different power supply domains. The three subblocks are supplied under 2.5 V. The different power supply pairs are written:

- VDDVCO/VSSVCO for the VCO
- VDDPh/VSSPh for the phase detector
- VDDDiv/VSSDiv for the frequency divider.

3 Principle of on-chip measurement

Three on-chip voltage sensors are placed on the VCO, the phase detector and the divider power supplies in order to characterize external interference coupling within the circuit PDN and extract the actual sensitivity level of each sub-block. The sensor is based on a wideband sample and hold (S/H) cell that directly probes the voltage on a given internal node without introducing any disturbances (Fig. 2) [2]. As shown on [3], the bandwidth of the sensor reaches 1.5 GHz.

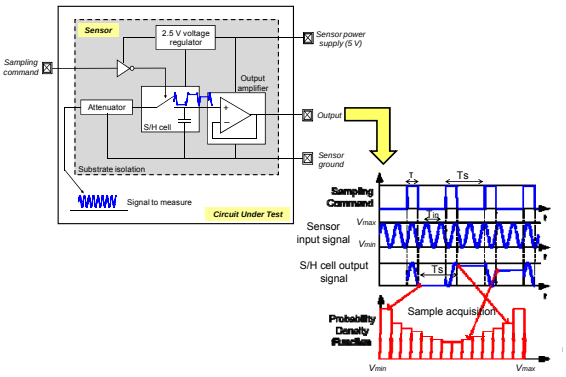


Figure 2: On-chip voltage sensor and random acquisition of conducted interference induced voltage fluctuation

The S/H cell is not synchronized on the external EMI so the acquisition of the internal voltage fluctuation is randomly performed and the time domain waveform cannot be reconstructed. But the statistical distribution of the voltage fluctuation, its amplitude and standard deviation can be extracted, which is enough since we want to characterize the peak-to-peak amplitude of voltage fluctuation induced by the interference coupling.

The on-chip sensor must be isolated from the disturbance applied on the sensed node. This isolation has been improved at both circuit and PCB design levels (separation of power supplies, decoupling, internal voltage regulation by a built-in regulator, substrate isolation).

4 Test board and set-up description

4.1 Board description

The circuit under test has been mounted on a 4 layer FR4 TEM board [4] developed by Freescale Semiconductor. At board level, the power supplies of PLL subblocks share the same 2.5 V internal power plane. The 2.5 V power planes is decoupled by a combination of one 47 µF electrochemical capacitors and eight 100 nF ceramic capacitors spread all over the test board. In the rest of the study, we will assume that the 2.5 V power plane is an equipotential.

However, the power supplies of PLL subblocks are isolated by 1.5 µH choke inductances placed between the 2.5 V power plane and individual power supply package pin. Package pins are connected to choke inductances by 0.7 mm wide and 16 mm long microstrip line. An additional 100 nF ceramic capacitor is added close to each power supply pin of PLL subblocks for a local decoupling. A SMA connector is placed at the input of the microstrip line for conducted interference injection, which is based on Direct Power Injection (DPI) standard [5]. The following figure illustrates the conducted interference coupling path at board level.

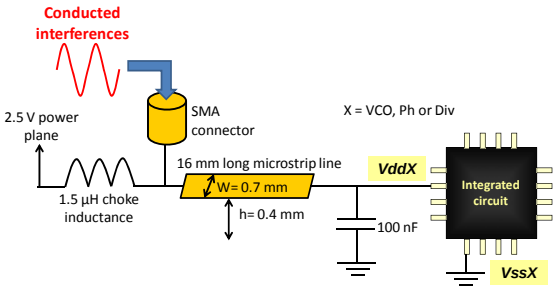


Figure 3: Schematic of conducted interference coupling path at board level

4.2 Conducted interference injection

The conducted interference injection is based on Direct Power Injection (DPI) standard [5] (report on chapter 7 for the principle and test bench description). The conducted injection relies on a bias tee made a DC block capacitor and a choke inductor. This inductor is directly on the test board. The DPI capacitor is external to the board and is a 6.8 nF X7R ceramic capacitor.

4.3 Test board modelling

From the previous information about the board, we can extract a passive equivalent model. For DPI and decoupling capacitors, a serial RLC model is proposed, based on

ESR (equivalent serial resistor) and ESL (equivalent serial inductance) values provided by the manufacturer: ESL = 0.6 nH and ESR = 25 mΩ. However, it is important to not underestimate the ESL, especially for the decoupling capacitor. For example, the decoupling capacitor is connected to the power supply and ground by small length of tracks and vias, which add parasitic inductances and resistances. ESL and ESR limit the decoupling efficiency which has a huge impact on the amount of conducted interference coupling. Initially, we decide to set the parasitic inductance of capacitor to 3 nH and the parasitic resistance to 100 mΩ.

The model of the choke inductance is extracted from VNA measurement. The model includes the 1.5 µH inductance with a serial resistor and a parallel capacitance which take into account the parasitic winding capacitances. This capacitance is required to reproduce the intrinsic resonance of this passive device. In order to reduce the sharpness of the resonance a large parallel resistance Rp is added, which models the loss in the inductor core.

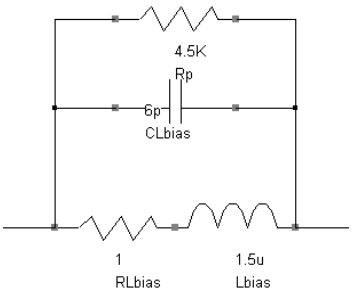


Figure 4: Equivalent passive model of the 1.5 µH inductor (1.5u_choke_inductance.sch)

Finally, the microstrip line model is extracted with the IC-EMC tool **Interconnects Parameters**. The characteristics of the board (FR4 material) and the geometrical dimensions of the microstrip are provided to build an equivalent electrical lumped model valid up to 1 GHz. Figure 5 presents the model of the injection path at board level, including the DPI capacitor.

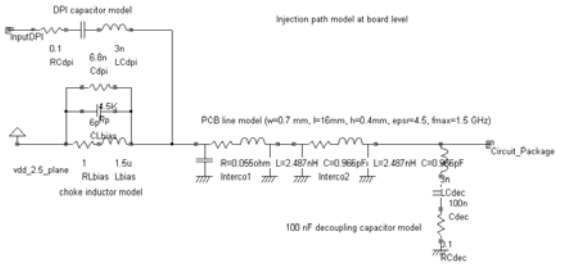


Figure 5: Electrical model of conducted interference coupling path at board level (PCB_injection_path.sch)

5 PLL PDN modeling by VNA measurements

The PDN of the PLL is made of three "sub-PDN" related to the power supplies of the VCO, the phase detector and frequency divider. (In the model proposed in the article [EMCCompo11], the PLL PDN also includes the PDN of the PLL I/Os. However, PLL and its I/O do not share the same power plane (I/Os are 5 V supplied) and a substrate separation isolate both blocks. As the coupling between the PLL PDN and I/O PDN is weak, we ignore I/O PDN in this case study for simplification purpose).

The PDN model of the PLL is an impedance network which links the power and ground pins of the PLL sub-blocks. Each sub-block counts one power supply and two ground pins. Moreover, the PLL input-outputs are biased by a dedicated power supply which can interact with the PLL PDN. Thus, the PLL PDN counts a total of 6 pins. (Actually, the PLL PDN includes 11 pins because 2 ground pins are used for the VCO, the frequency divider and the phase detector. With the I/O power supply and ground pins, the total number of considered pins is equal to 11. Here, we only consider one ground pin per block in our model for simplification reason).

A specific test board has been designed to extract the impedance network of the PLL PDN by 2-port S parameter measurements. The circuit is connected to a vector

network analyzer (VNA) by high frequency GS probes (Fig. 6). Probes are connected to PCB pads placed as close as possible to the circuit under test. All the measurement configurations between each pin of the PLL PDN are possible, so package inductances, block equivalent capacitances, substrate coupling … can be extracted from measurements. Moreover, the ground pins can be connected or not to the test board ground plane in order to extract the interaction between the die and the test board.

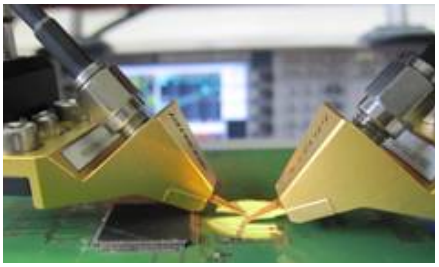


Figure 6: PLL PDN model extraction by S parameter measurements [1]

A large number of 2 ports measurements have been done between the 6 pins of the PLL PDN. The measurements show that:

- The equivalent impedance between the power supply and the ground of one block (VCO, frequency divider, phase detector) is capacitive. This equivalent capacitance resonates with package inductance.
- The different ground pin is resistively coupled by the substrate. Between the ground pins of each block, a resistor about 17 – 20 Ω is measured. As these different blocks share the same P+ substrate, a significant substrate coupling exists between their ground connections.
- A capacitive coupling also exists between each ground pin and the ground of the test board. It is a direct coupling between the circuit substrate (or the die) and the printed circuit board.
- Although the power supply rails of the different subblocks are internally separated, they are not isolated perfectly. A small capacitive coupling appears. VddVCO, VddDiv and VddPh are coupled with the I/O power supplies in the I/O and ESD structures.

The structure of the equivalent model of the PDN is proposed from these observations. The electrical elements and their values are then fitted from the measurements. The following figure presents the PLL PDN model. The different part of the PDN model has been separated.

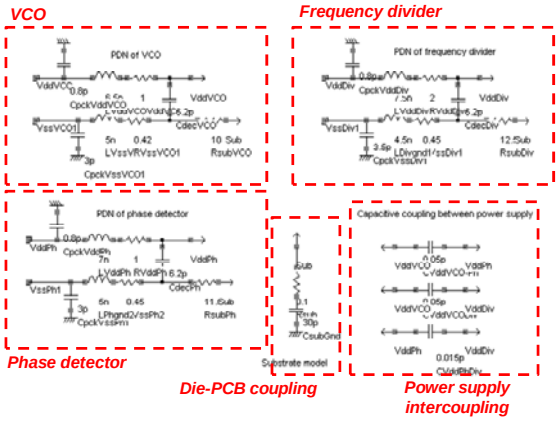


Figure 7: Equivalent electrical model of PLL PDN extracted by S parameter measurements

Some of these measurements are provided with this case study to show the previous observations and evaluate the accuracy of the model. The following figure presents the model used to simulate the 2 port S parameter measurements between VddVCO and VddPh, when all the ground pins are shorted to the ground (S2P_VddVCO_VddPh_gnd_0ohms.sch). Two port symbols have been placed on VddVCO and VddPh terminals and the ground terminals have been shorted to the ground.

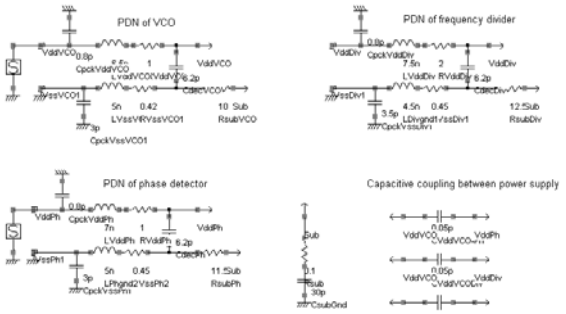


Figure 8: Model for the simulation of 2 port S parameter measurements between VddVCO and VddPh (S2P_VddVCO_VddPh_gnd_0ohms.sch)

The simulation results are compared with measurements in Touchstone format (see Appendix A of User's Manual for more information about Touchstone file) in the **S parameter** tool . The measurement result is given in the file s2p_VddVCO_VddPh_gnd0ohm.s2p. The following figure compares the simulated and measured Z11 parameter seen from the VddVCO terminal. The input impedance is mainly capacitive due to the equivalent on-chip capacitance of the VCO. A resonance appears about 600 MHz due to package inductance and on-chip capacitance of the VCO. The measurement quality in low frequency seems degraded because the VNA measures large impedance. But a S11 measurement is not the best adapted method to measure high impedance. The quality degradation happens because the dynamic of the VNA is not infinite.

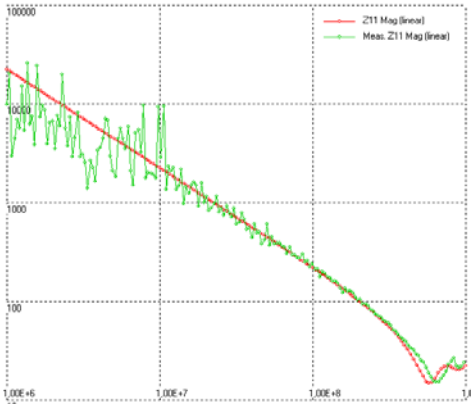


Figure 9: Comparison between simulated and measured Z11 seen from VddVCO (S2P_VddVCO_VddPh_gnd_0ohms.sch and s2p_VddVCO_VddPh_gnd0ohm.s2p)

In the next figure, the simulated and measured transmission coefficient S12 between VddVCO and VddPh are compared. Ideally, the isolation between these power supplies should be perfect. Actually, it is true only below 200 MHz. Above 250 MHz, the coupling is not negligible since the transmission coefficient exceeds 30 dB. The consequence is that if the VCO power supply is disturbed, a part of the disturbance will be coupled on the phase detector power supply. The correlation between measurement and simulation is not perfect and it is difficult to improve it with this model. However, the model succeeds in representing this coupling with the good order.

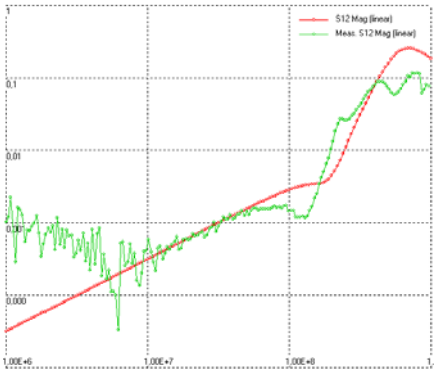


Figure 10: Comparison between simulated and measured S12 seen between VddVCO and VddPh (S2P_VddVCO_VddPh_gnd_0ohms.sch and s2p_VddVCO_VddPh_gnd0ohm.s2p)

The next figure presents the model used to simulate the 1port S parameter measurement from VssVCO, when all the other ground pins are shorted to the ground (S1P_VssVCO_ gnd_0ohms.sch). A port symbol has been placed on VssVCO terminal and the other ground terminals have been shorted to the ground. These simulation and measurements aim at extracted the impedance connected between the ground pins, and especially the equivalent resistance of the substrate coupling.

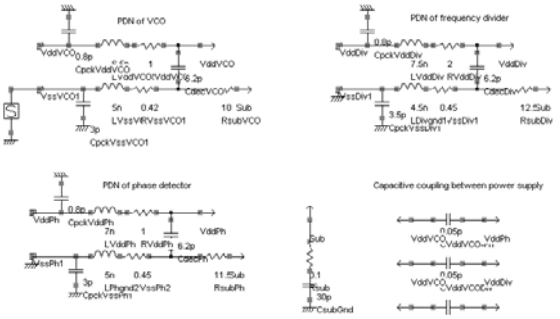


Figure 11: Model for the simulation of 1 port S parameter measurement from VssVCO (S1P_VssVCO_gnd_0ohms.sch)

The measurement result is given in the file s1p_VssVCO_gnd0ohms.s1p. The following figure compares the simulated and measured Z11 parameter seen from the VssVCO terminal. The input impedance is mainly resistive up to 100 MHz due to the substrate coupling. Above 100 MHz, the inductive effect of package pin appears. The correlation is not perfect above 100 MHz and the inductance seems to be underestimated, because the ground pin model has been simplified.

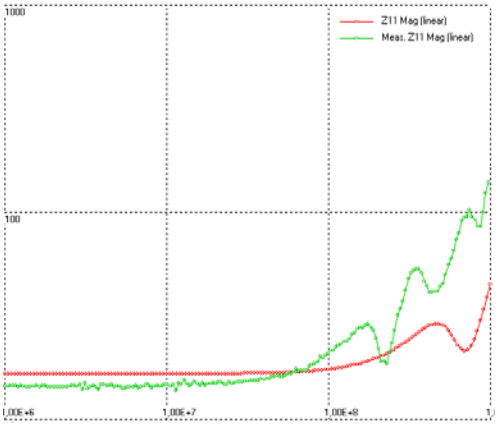


Figure 12: Comparison between simulated and measured Z11 seen from VssVCO (S1P_VssVCO_gnd_0ohms.sch and s1p_VssVCO_gnd0ohms.s1p)

The next figure presents the model used to simulate the 2 port S parameter measurement between VssVCO and VssPh, the pin VssDiv is opened (S2P_VssVCO_ VssPh_gnd_open.sch). Two port symbols have been placed on VssVCO and VssPh terminals. The simulation and measurement of Z12 parameter aim at extracted the parallel impedance connected between these two ground pins, which is mainly due to the coupling between the die and the test board.

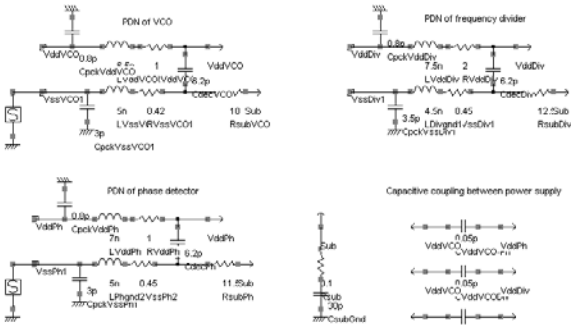


Figure 13: Model for the simulation of 2 port S parameter measurements between VssVCO and VssPh (S2P_VssVCO_VssPh_gndOpen.sch)

The measurement result is given in the file s2p_VssVCO_VssPh_gndOpen.s2p. The following figure compares the simulated and measured transfer impedance Z12 parameter between VssVCO and VssPh terminals. The parallel impedance between both terminals is mainly capacitive and is due to both package pin to the test board ground and die to the test board ground capacitances.

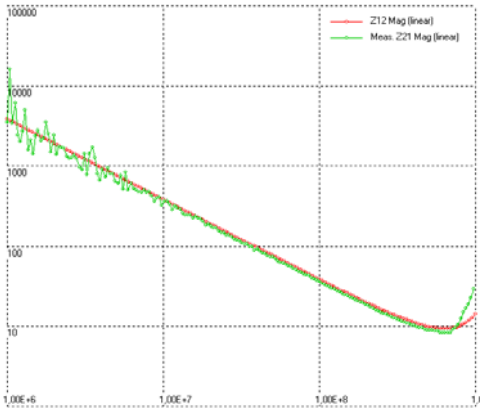


Figure 14: Comparison between simulated and measured Z12 seen between VssVCO and VssPh (S2P_VssVCO_VssPh_gndOpen.sch and s2p_VssVCO_VssPh_gndOpen.s2p)

6 Validation of PDN modeling by the measurement of conducted interference coupling

The model presented in the previous part is able to reproduce the impedance profile seen from any terminals of the PLL PDN. However, is this model able to reproduce the coupling of an external conducted disturbance within the circuit? In other words, for a given conducted disturbance (i.e. a known forward power at a given frequency when the circuit immunity is tested using a DPI test bench), can we predict accurately the amplitude of the voltage fluctuation on a given internal node of the circuit? This is a critical point since susceptibility of a circuit is directly related to the amount of voltage fluctuation induced across sensitive nodes.

In this part, we will focus our study on the conducted disturbance of the VddVCO pin. To answer to the previous question, we will compare measurements and simulations of the voltage fluctuation induced on the internal power supply terminal of the VCO.

6.1 Conducted interference coupling transfer function

As seen in the previous part, the impedance profile of the PLL PDN is frequency dependent, so that the PLL PDN is equivalent to a frequency dependent filter of the voltage fluctuation induced by the conducted EMI. The filtering effect can be expressed by a transfer function that relates the induced voltage fluctuation ΔV to the amount of incoming disturbance. In DPI test, the conducted disturbance amount is given in term of forward power P_{forw}. We define the conducted interference coupling transfer function H_{EMI} to characterize the filtering effect of a conducted interference by an impedance network such as the PLL PDN.

Let's suppose that the PDN is modeled by an impedance matrix with the first port placed on the node where the voltage fluctuation is measured (across a sensitive function of the circuit) and the second port placed at the injection node.

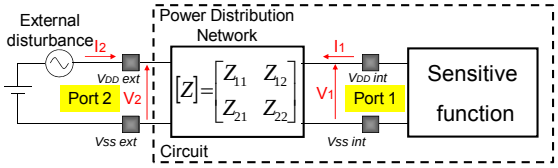


Figure 15: Analysis of the coupling of an external conducted disturbance to an internal node of a circuit

In the following analysis, we are only focused on the voltage fluctuations V1 across the IC sensitive function when an external disturbance expressed in term of current i2 is coupled on the power supply. The current resulting from the internal activity of the circuit i1 is not considered here. The internal power supply voltage fluctuations V1 is linked to RF current i2 induced by the external disturbances by the transfer impedance parameter Z_{12}, as shown in equation 1. The internal power fluctuation v_1 can be related to external voltage fluctuations v_2 by introducing the input impedance Z_{22} seen between the external power supply pins (equation 2).

$$Z_{12} = \left.\frac{v_1}{i_2}\right|_{i1=0} \quad \textit{Equation 1}$$

$$Z_{22} = \left.\frac{v_2}{i_2}\right|_{i1=0} \Rightarrow \left.\frac{v_1}{v_2}\right|_{i1=0} = \frac{Z_{12}}{Z_{22}} \quad \textit{Equation 2}$$

The ratio V_1/V_2 expresses the external noise coupling across the sensitive function. It can be reduced by minimizing the ratio Z_{12}/Z_{22}. During conducted immunity tests, immunity levels are usually expressed in terms of power of the forward wave. The voltage (V_{forw}) and the power of the forward wave (P_{forw}) are related to V_1 by the following relations:

$$\left.\frac{v_1}{v_{forw}}\right|_{i1=0} = \frac{2.Z_{12}}{Z_C + Z_{22}} \quad \textit{Equation 3}$$

$$\left.\frac{v_1}{p_{forw}}\right|_{i1=0} = \frac{4.Z_{12}^2 Z_C}{(Z_C + Z_{22})^2} \quad \textit{Equation 4}$$

Zc is the characteristic impedance of the injection system. The immunity of a circuit can be improved if the internal voltage fluctuation is reduced for a given forward power. It can be obtained by minimizing the Z_{12} parameter and/or increasing the Z_{22} parameter.

If the input impedance Z_{22} is negligible compared to the characteristic impedance Zc (usually equal to 50 Ω), equations 3 and 4 can be rewritten, and the internal noise coupling depends only on the Z_{12} parameter.

$$\left.\frac{v_1}{v_{forw}}\right|_{i1=0} = \frac{2.Z_{12}}{Z_C}, Z_{22} << Z_C \quad \textit{Equation 5}$$

$$\left.\frac{v_1}{p_{forw}}\right|_{i1=0} = \frac{4.Z_{12}^2}{Z_C}, Z_{22} << Z_C \quad \textit{Equation 6}$$

The conducted interference coupling transfer function is given by the ratio V_1 on P_{forw}. It is strongly correlated with the impedance profile of the PDN.

$$H_{EMI}(f) = \frac{4.Z_{12}^2 Z_C}{(Z_C + Z_{22})^2} \quad (V/W) \quad \textit{Equation 7}$$

The unit of this function is V/W. It gives the amount of forward power of a conducted disturbance to induce a given voltage fluctuation. It quantifies the efficiency of coupling of the conducted disturbance on a node at a given frequency.

6.2 Measurement of conducted interference coupling transfer function

In order to characterize the conducted interference coupling transfer function of the PLL PDN to conducted injection on VCO power supply, the internal sensor placed on the VCO power supply is used to measure voltage fluctuation induced during DPI test. The experimental test set-up is described in the figure 16 [1]. For different frequencies ranging from 1 MHz to 1 GHz, harmonic disturbances are generated and conducted to the VddVCO pin. For each frequency, the forward power of the disturbance is set to induce a given internal voltage fluctuation, measured by the on-chip sensor. The amplitude of the voltage fluctuation should be large enough to ensure an accurate measurement, but not too large to ensure small signal conditions. The amplitude is set to 0.25 V.

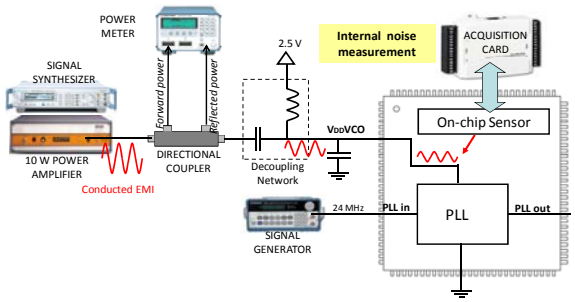


Figure 16: Experimental set-up to measure the conducted interference coupling transfer function [Boyer11]

The following figure presents the experimental results. The conducted interference coupling transfer function measured internally by the sensor is compared with the one measured externally with an oscilloscope active probe placed on the VddVCO package pin. The active probe is given up to 2.5 GHz. Ideally, both measurements should give the same result because the same node is probed (the power supply of the VCO). However, this ideal vision ignores the impedance between the 2 measurement points: package inductance, I/O pads, IC interconnects… which explains the difference observed between both measurements above 100 MHz.

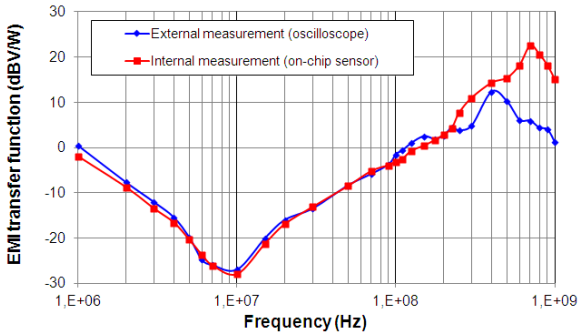


Figure 17: Comparison of EMI transfer function of VCO power supply pin measured internally and externally [1]

6.3 Simulation of conducted interference coupling transfer function

In order to simulate the conducted interference coupling transfer function, a model including the DPI injection system, the test board and the circuit PDN has to be developed. This model is described in figure 18.

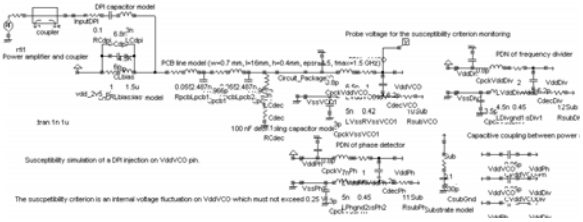


Figure 18: Model for the simulation of the conducted interference coupling transfer function based on susceptibility simulation (DPI_VCO_Vdd.sch)

In IC-EMC, two methods exist to simulate the conducted interference coupling transfer function:

- A typical susceptibility simulation (see chapter 7), based on iterative transient simulation and a definition of susceptibility criterion
- As this transfer function is related to impedance parameters, it can be calculated directly from S parameter simulation results

We will present both methods.

6.3.1 Simulation method 1 – Susceptibility simulation

With this method, the forward power required to reach a given voltage fluctuation is computed over a frequency range. Several elements are added in the model to perform this simulation:

- The power amplifier, modeled as sinusoidal voltage source with a serial output resistance equal to Ω
- The coupler, modeled as a lossless transmission line, which ensures the forward power extraction
- A voltage probe for the susceptibility criterion monitoring. In this case study, it is reached when the voltage fluctuation amplitude across the VCO power supply exceeds 0.25 V.

A transient simulation is configured. Click on the icon  to open the susceptibility simulation control screen. The following figure describes the configuration of susceptibility simulation for the frequency range [1 – 10 MHz]. The general parameters of the simulation are:

- the frequency sweeping is logarithmic (15 points per decade) between 1 and 100 MHz
- the maximum forward power is set to 50 dBm
- a failure is detected if the voltage VddVCO exits the range [2.25 V; 2.75 V] (select ), which indicates a voltage fluctuation amplitude larger than 0.25 V.
- the simulation result is ignored during the first 10 ns period to ensure a convergence of transient simulation
- the simulation control file is called 'RFIcontrol_DPI_VCO_Vdd.ctl'

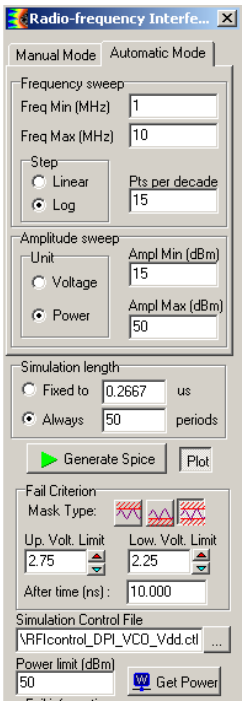


Figure 19: Configuration of the susceptibility simulation for the frequency range 1 – 10 MHz

However, the configuration of RFI source amplitude sweep and the transient simulation duration are more delicate. The accuracy of the extraction of the susceptibility threshold relies on a slow increase of disturbance level which has to lead to a failure (see chapter 7 of User's Manual).

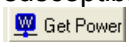
The measurement of conducted interference coupling on VddVCO, seen in figure 17, shows that the susceptibility threshold of the circuit evolves very rapidly with frequency: more than 30 dB per decade. If a unique configuration for susceptibility simulation is used, the accuracy of the susceptibility extraction is difficult to ensure over the full frequency range.

Actually, the accuracy can be improved if the frequency range is divided in several intervals, for example per decade. A unique configuration is defined on each frequency interval. Table I gives the configuration for RFI source amplitude sweeping and transient simulation duration. The amplitude sweeping has been optimized to reduce its excursion. The simulation duration is given in terms of RFI periods in order to reduce the simulation length for higher frequency. For example, at 1 MHz, the simulation duration is equal to 50 periods, i.e. 50 µs, while it lasts 5 µs at 10 MHz. But, for a given amplitude sweeping, the longer the simulation, the more accurate is the susceptibility level extraction.

Frequency range	RFI source amplitude sweeping	Transient simulation duration
1 – 10 MHz	20 – 50 dBm	50 periods
10 – 100 MHz	20 – 50 dBm	100 periods
0.1 – 1 GHz	-15 – 25 dBm	200 periods

Table 1: Configuration of RFI source amplitude sweeping and transient simulation duration

Click on the button 

to generate the SPICE netlist and then launch the WinSPICE simulation. The simulation can take one or two minutes since 46 transient simulation have to be done (the time necessary to find the best simulation configuration should be added to the total simulation time). At the end of WinSPICE simulation, enter '0.25' in the field "Up Voltage Limit" to set the susceptibility criterion. Click on the button 

to extract the susceptibility limit in term of forward power. The simulation result is displayed on the graph on the right. It is the required forward power to induce a 0.25 V voltage fluctuation across VddVCO within the circuit. To compare this result with the measurement, click on the button 

and select the file PLL_internal_PDN_0.25V_coupling.tab. This file contains the measurement result data in the format (frequency; forward power (dBm)) of figure 17. Figure 20 presents the comparison between the measurement and simulation of the susceptibility threshold of the PLL to conducted disturbances (the susceptibility criterion is the induction of: 0.25 V voltage fluctuation induced across VddVCO). The simulated susceptibility threshold has been saved in the file "DPI_VCO_Vdd_susceptibility_threshold.tab".

The correlation between measurement and simulation is quite good, except around:

- 1 MHz because of the loss of accuracy of susceptibility threshold extraction at low frequency
- 600 MHz because of some simplification provided to the circuit model

However, this comparison proves that the PDN model ensures a good prediction of conducted disturbance coupling within the component on the VCO power supply. This simulation method is not very efficient in term of simulation time. As the model is purely passive and linear, we can test a second simulation approach based on an AC simulation and Z parameter computation.

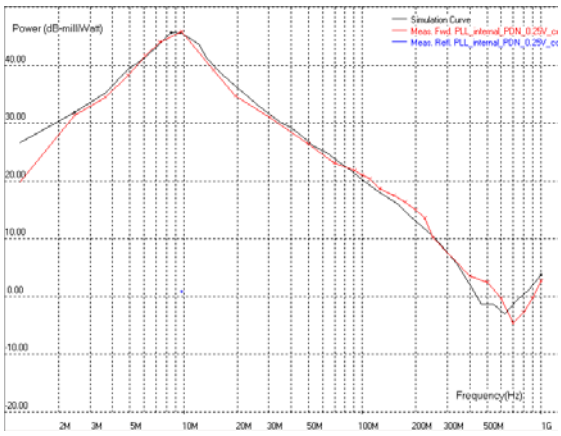


Figure 20: Comparison between measurement (PLL_internal_PDN_0.25V_coupling.tab) and simulation (DPI_VCO_Vdd.sch) of the susceptibility of the PLL to conducted disturbances (criterion: 0.25 V voltage fluctuation induced across VddVCO)

6.3.2 Simulation method 2 – S parameter simulation

This method is based on the equation 9, and requires a preliminary Z parameter calculation. Thus, it only requires a AC simulation, which takes only few seconds. This method is really faster compared to the previous one which requires a large number of transient simulations. However, the limit of this method is the necessity to ensure small signal conditions.

In the previous SPICE model (DPI_VCO_Vdd.sch), the voltage probe used to monitor the susceptibility criterion is replaced by S parameter port, named 1. The RF source and the coupler are replaced by a second S parameter port, named 1. The transient simulation command is replaced by the following AC simulation command: ".AC DEC 50 1MEG 1G". The new model file is called EMI_TF_VCO_Vdd.sch and is presented below.

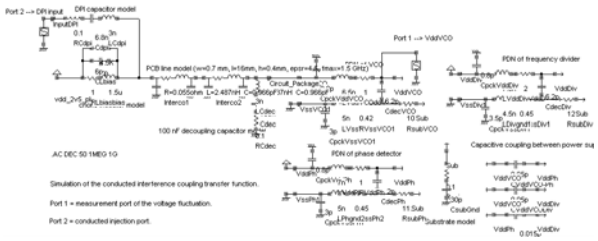


Figure 21: Model for the simulation of the conducted interference coupling transfer function based on S parameter simulation (EMI_TF_VCO_Vdd.sch)

Click on  to generate the SPICE netlist and launch WinSPICE simulation. At the end of the simulation, open the **S parameter** tool  to display the result. In the S parameter List, select 'EMI Tranf Funct (V/W)'. Select 'Mag (dB)' in the Format List and write 0.25 in the field 'Voltage (V)'. Finally, click on the button Add to display the conducted interference coupling transfer function.

Figure 20 presents the simulation results given in dBV/W. This result can be compared with the measurement result presented in figure 17. Some markers have been added on the simulation result for comparison purpose. The simulation result follows the same trend. The difference between measurement and simulation results is less than 3 dB. This difference can be explained by some simplifications made in the model compared to the original model [1].

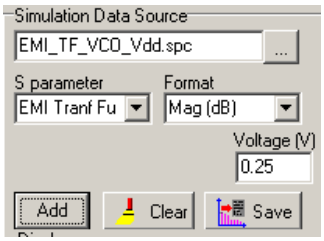


Figure 22: Display the conducted interference coupling transfer function

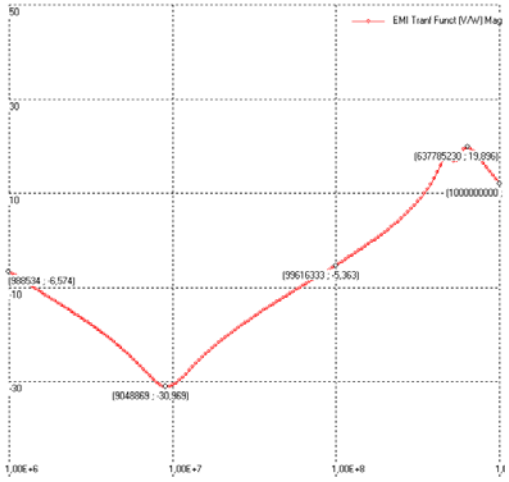


Figure 23: Simulated conducted interference coupling transfer function (EMI_TF_VCO_Vdd.sch). Compare with measurement result in figure 17

Once again, this result proves the relevance of the circuit PDN model extracted by S parameter measurement to predict accurately the amount of voltage fluctuation within the circuit induced by the coupling of an external conducted interference.

6.4 Discussion about conducted interference coupling on VCO power supply

The conducted interference coupling transfer function quantifies the efficiency of the conducted interference coupling on the VddVCO node for a given frequency. For example, the interference coupling is the less efficient at 10 MHz, where the transfer function is equal to -30 dBV/W. It means that, in a DPI test similar to the test that we have performed, a forward power equal to 30 dBW (60 dBm !) is necessary to induce a voltage fluctuation equal to 1 V on VddVCO.

Inversely, the coupling of the conducted disturbance is particularly efficient about 600 MHz, where the measured transfer function is equal to 20 dBV/W. It means that a forward power equal to -20 dBW (10 dBm) is required to induce a voltage fluctuation equal to 1 V on VddVCO.

Simulation or measurement results show that the disturbance coupling efficiency has a frequency dependent behavior which changes rapidly with the frequency. Can we explain the origins of these variations? Equation 9 can help us to answer to this question. Even if our model is quite complex, it can be simplified, as shown in figure 24 (the DPI capacitor is a low impedance over the range 1 – 1000 MHz, so it has been replaced by a short circuit). This simple model can help to predict rapidly what is the efficiency of conducted interference coupling on VddVCO node at board level.

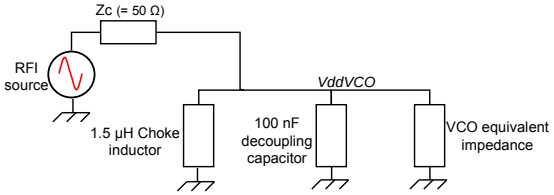


Figure 24: Equivalent model of conducted injection on VddVCO

The RF source is connected to 3 parallel loads:

- the choke inductance (followed by the 2.5 power plane that we suppose to be a low impedance), which is a high impedance over all the considered frequency range. Its impedance profile is shown in figure 25.
- the 100 nF decoupling capacitor, which is very efficient about 10 MHz. Thus, it is a low impedance between 1 MHz and some hundreds of MHz. Its impedance profile is shown in figure 25.
- the equivalent impedance seen between the VCO power supply pin

and the board ground (see figure 8 for the comparison between measured and simulated impedance seen from VCO power supply). Globally, it is high impedance, except around 600 MHz.

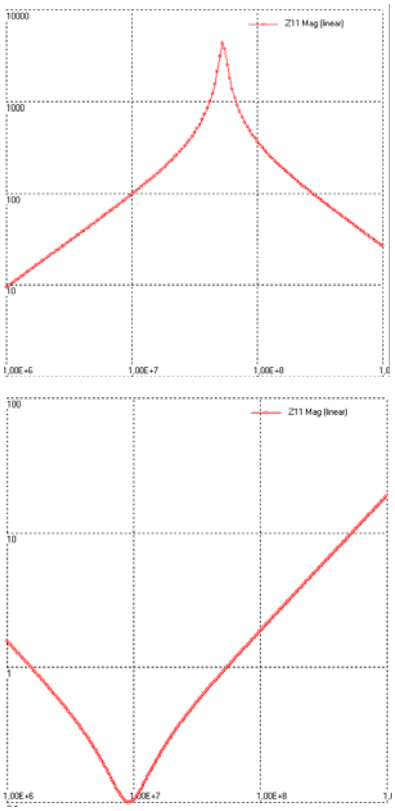


Figure 25: Simulated impedance profile of 1.5 µH inductor (1.5u_choke_inductance.sch) (top) and 100 nF decoupling capacitor (100nF_decoupling.sch) (bottom)

The coupling of the conducted disturbance on VCO power supply at board level depends on the impedance of this node. If one of the three previous elements has a very low impedance at a given frequency, then the conducted interference coupling transfer function is very small, since the low impedance acts as a decoupling. A very small voltage fluctuation is induced. Conversely, if the three elements form a large impedance, the conducted interference coupling transfer function is high and a significant voltage fluctuation can be induced for a given amount of conducted disturbance.

The conducted disturbance coupling is strongly dependent on the board characteristics. Let's simulate the conducted interference coupling transfer function on VddVCO node without the PLL. Open the file 'PCB_injection_path_coupling.sch', where the PLL PDN model has been removed (figure 26). Figure 27 presents the simulation result of the conducted interference coupling transfer function. The transfer function is similar to the transfer function of the full model (see figure 23), except above 400 MHz where the circuit has an influence. This result shows clearly both the role of decoupling capacitor around 10 MHz, where it ensures a very low impedance and an efficient decoupling, and the choke inductor which can ensure a high impedance except above 700 MHz where its impedance becomes enough small to reduce noise coupling. The parasitic parallel capacitor of the inductor can short circuit a part of the conducted interference to the 2.5 V power plane, which can decouple this interference if it is carefully designed.

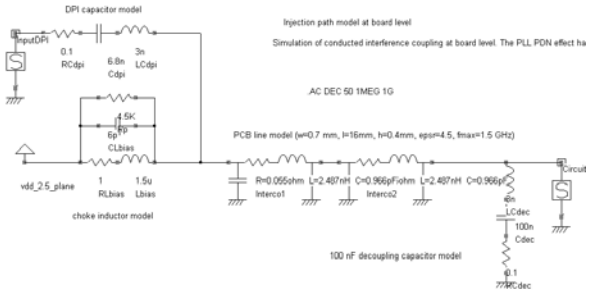


Figure 26: Model for the simulation of conducted interference coupling on VddVCO at board level, without the effect of the PLL PDN (PCB_injection_path_coupling.sch)

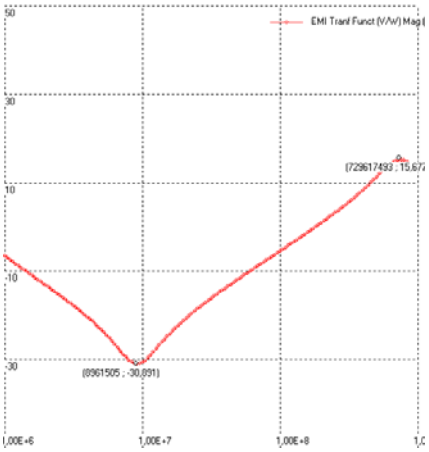


Figure 27: Simulation of conducted interference coupling on VddVCO at board level, without the effect of the PLL PDN (PCB_injection_path_coupling.sch)

The contribution of the PCB and external devices is predominant over all the frequency range. So, what is the contribution of PLL PDN? As shown in figure 9, the impedance seen from VddVCO is high impedance, except around its resonant frequency at 700 MHz. At this frequency, the VCO on-chip capacitor resonates with power supply and ground package inductance so that the circuit impedance is the lowest. Thus it can have an influence on the conducted interference coupling on VddVCO at board level.

The resonance of VCO on-chip capacitor with package inductance has another consequence. In this case study, we are focused on the voltage fluctuation induced within the circuit. It depends not only on the efficiency of conducted interference to couple at board level (i.e to produce a large voltage fluctuation on VddVCO node at board level), but also on the transfer of the external voltage fluctuation within the circuit. The following schematic (TF_VddVCO_out-in.sch) is used to simulate the transfer function between the internal and external VddVCO node. Both nodes are separated by VddVCO package pin and circuit interconnects. The model reuses the PLL PDN model presented in figure 7. An AC 1V voltage source is added at the input of VddVCO package pin, and a voltage probe is placed across the on-chip capacitance of the VCO.

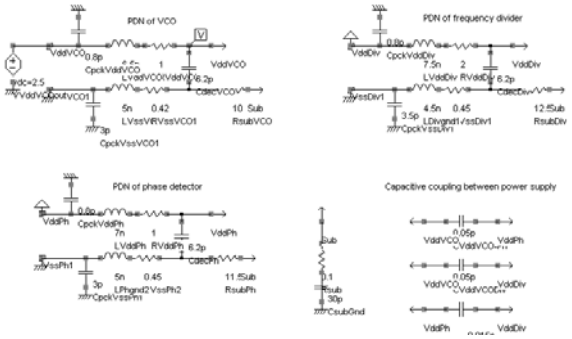


Figure 28: Model for the simulation of the transfer function between the internal and external VddVCO node (TF_VddVCO_out-in.sch)

An AC SPICE simulation is configured and launched. WinSPICE displays the following results shown in figure 29. Between 1 and 200 MHz, the package has no significant influence and the same amount of voltage fluctuation is observed inside or outside the circuit along VddVCO (it is confirmed by the external and internal noise measurements presented in figure 17). Above 200 MHz, the voltage fluctuation inside the circuit exceeds the one measured outside the circuit, especially around 700 MHz (it is also confirmed by the comparison between external and internal measurements of voltage fluctuation presented in figure 17). On-chip VCO capacitance and power supply and ground package pin inductances form a second order filter placed along VddVCO, which produces an anti-resonance at 700 MHz (a smaller antiresonance is also observed at 500 MHz, because of the complexity of ground network of the circuit. Three ground pins are interconnected by substrate, which is also capacitively coupled to the PCB ground). If an external disturbance excites this filter at 700 MHz, the on-chip voltage fluctuation on VddVCO is optimized. Taking into account the circuit effect has a major importance above 200 MHz to predict accurately the amount of on-chip voltage fluctuation, which is larger than the voltage fluctuation measured on-board.

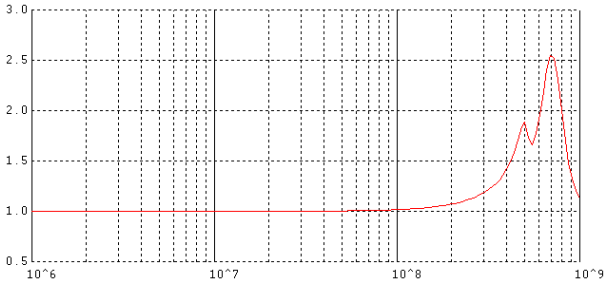


Figure 29: Simulation of the transfer function between the internal and external VddVCO node (TF_VddVCO_out-in.sch)

Ideally, the circuit antiresonance should be sharper. But the PLL PDN is more complex than a simple LCL filter. We can wonder if it matters if we use a simpler model for the PLL PDN, which takes only into account the VCO PDN and ignores substrate coupling between VCO, phase detector and frequency divider ground pins, and the capacitive coupling between the die and the PCB ground. In other words, must we care about the circuit PDN modeling or must we only focus on a precise board modeling (as suggested by simulation result presented in figure 27)?

The answer is “no”, especially at the circuit resonance (above 200 MHz). If the structure of ground network is ignored, the antiresonance of the circuit cannot be accurately modeled and the on-chip voltage fluctuation cannot be precisely predicted. In order to prove this affirmation, let’s build a simpler PLL PDN model where we assume that there is perfect substrate isolation and no capacitive coupling exists between the die and the PCB ground plane. The model called ‘EMI_TF_VCO_Vdd_PDN_simple.sch’ is proposed for this simulation (figure 30). Figure 31 presents the simulation result of the conducted interference coupling transfer function. This simulation result can be compared with the simulation result obtained with the full PLL PDN model presented in figure 23, and the measurement presented in figure 17. Both models give similar result up to several hundreds of megahertz. However, the simple model is not able to provide an accurate prediction of the on-chip voltage fluctuation. The substrate coupling tends to modify the inductance between the VCO and the PCB ground plane. Moreover, the die to PCB capacitance tends to short circuit the inductive ground path between VCO and PCB ground plane. These effects have a significant influence at anti-resonant frequency and thus have to be taken into account.

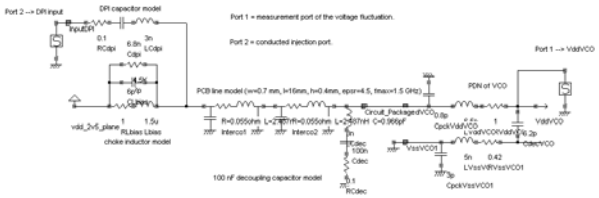


Figure 30: Model for the simulation of a conducted injection on VddVCO, with a very simple model of PLL PDN (only VCO PDN is taken into account, substrate coupling is ignored) (EMI_TF_VCO_Vdd_PDN_simple.sch)

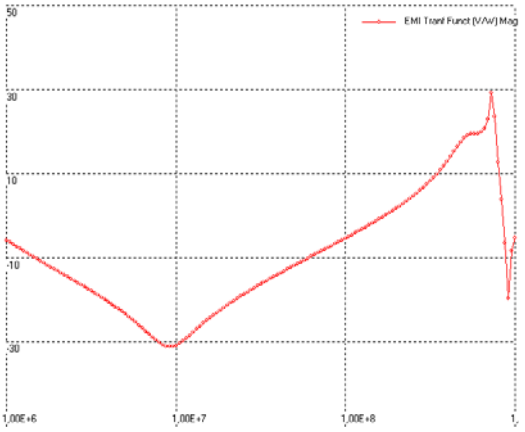


Figure 31: Simulation of a conducted injection on VddVCO, with a very simple model of PLL PDN (EMI_TF_VCO_Vdd_PDN_simple.sch)

7 Conclusion

The susceptibility of a circuit is strongly related to the propagation of interferences up to circuit terminals. This case study has been focused on the modeling of an external conducted interference coupling within an integrated circuit. The equivalent passive model of the power distribution network (PDN) of a phase-locked loop has been extracted from S parameter measurements. The model includes the

individual PDN of each subblock of the PLL, the intercoupling between them, and a direct capacitive coupling between the die and the test board ground plane. A combination of conducted immunity test and on-chip voltage measurement has been performed to characterize the efficiency of an external disturbance to induce an on-chip voltage fluctuation between 1 and 1000 MHz. The model has succeeded in reproducing this measurement up to 1 GHz, with two different simulation methods proposed by IC-EMC (based on AC and transient simulations).

The notion of conducted interference coupling transfer function has been introduced and linked to the impedance profile of PDN to analyze the frequency dependent behavior of interference coupling in the circuit. The analysis has shown that the PCB has a predominant impact up to some hundreds of megahertz, but the circuit starts to have a major impact on noise coupling above some hundreds of megahertz. The on-chip resonance between circuit equivalent capacitance and package pin inductance produces resonances and anti-resonances which can influence the amount of induced voltage fluctuation considerably. The intercoupling between other circuit blocks, such as substrate coupling) or the coupling between die and PCB ground plane have to be carefully modeled to predict the frequency and the level of these resonances.

References

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